Aligned GaAs Pillar Bonding

by

Donald S. Crankshaw

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ABSTRACT

A method was developed to bond pillars patterned on one GaAs substrate into wells patterned on another GaAs substrate which also contained VLSI circuitry. This required the use of an infrared backside aligner to achieve a 10 μm tolerance alignment. Bonding was performed at a temperature of 530°C, low enough to prevent significant damage to the metal contacts or the electronics. The substrate was removed by first flowing resist into the region between the two substrates and then etching away the substrate into which the pillars were etched.

Results obtained from this procedure and from other tests involving bonding pillars on flat surfaces indicated strong mechanical adhesion and good electrical contact between the substrates. Deformation was observed on both substrates due to dislocation motion resulting from the high pressures at the interface.

Thesis Supervisor: Clifton Fonstad
Title: Professor of Electrical Engineering

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Table of Contents

Acknowledgements 5

Table of Contents 7

Table of Figures 9

1 Introduction 13
- The OPTOCHIP project 13
- Thesis Outline 14

2 Wafer Bonding 17
- Wafer bonding 17
- Epitaxial Lift Off 17
- Palladium bonding 20
- Wafer fusion 22
- Mass Transport 26
- Dislocation Motion 27

3 Experimental Setup 33
- The Furnace 33
- Unpatterned Samples 35
- Patterned Samples 36
- Aligned Bonding 38

4 Results 47
- Unpatterned Samples 47
- Pillar Bonding 52
- Comparison of Electrical Characteristics of Flat and Patterned Wafers 61
- Aligned Wafer Bonding 64

5 Conclusions 73
- Project Summary 73
- Devices 74
- Palladium bonding revisited 76

A.I Bibliography 79

A.II Sample Database 81

Table of Figures

Figure 1-1. The chip created by the OPTOCHIP foundry. The chip is made up of nine patterns created by different groups. They consist of electronic circuits and wells into which optical devices are grown. In this project, the possibility of bonding devices into the wells is explored. (Photograph courtesy of Joseph Ahadian) 14

Figure 2-1. Thin film lifted off and transplanted onto new substrate. Wax protects the sides of the thin film during the etch which removes it and also provides support as it is transferred. This technique was used in the work of Chan *et al.*[6] 18

Figure 2-2. Propagation of a light-wave in the ELO bonded samples. The light coupling across the ELO bond is tested by measuring the loss in the guiding layer.[6] 19

Figure 2-3. ELO bonded sample under TEM. A layer of low refractivity material, which prevents significant light coupling across the bond, is apparent.[6] 19

Figure 2-4. TEM of a palladium bond accomplished in a similar manner to ELO and annealed at 200°C. There is no discernible barrier layer.[8] 21

Figure 2-5. Liau's wafer fusion setup. The difference in thermal coefficients of expansion causes the graphite to expand more quickly than the quartz tube it is in. The exerts pressure on the wafers, causing them to fuse under the pressure and the heat. The graphite shim is used to get correct spacing for wafers of different thicknesses.[1] 22

Figure 2-6. I-V curves of p-GaAs/p-InP bonded at various temperatures, as determined by Wada *et al.*[5] The structure is essentially a diode at low bonding temperatures, but becomes more linear with higher temperatures. 25

Figure 2-7. Lattice potential energy between two atoms in the crystal. It is approximated as sinusoidal. The force resisting movement is highest at a/4, where the slope is steepest. The resistance becomes very high when a whole plane of atoms must overcome a similar force. 28

Figure 2-8. The beginning point of the halfplane dislocation is shown in (a). It can propagate through the material, one plane at a time, until it reaches (b), the end point of halfplane, at the surface of the material. 29

Figure 2-9. A Frank-Read source. A dislocation starts out as a straight line between two impurities which anchor it (a). This prevents the end points from moving, causing the halfplane to bend under pressure (b). Its total curvature is limited, causing it to loop back (c and d). Eventually the back loops intersect (e), creating a complete loop of dislocations (f) and a new line (a) which repeats the process. 30

Figure 3-1. Diagram of the furnace plumbing. It shows the flow of N_2 and H_2 gases within the system. (From the LPE manual written by Peter Whitney.) 34

Figure 3-2. Furnace profile for a 625°C bonding run. Both the boat temperature (T1), and the furnace temperature (T2), show good agreement with the set temperature, except near the end where the exponential decay of the temperature is slower than the linear ramp rate. 34

Figure 3-3. Wells in the OPTOCHIP, prior to cleaning. A top layer of SiO_2 must be removed, followed by a layer of Al, more SiO_2, and finally SiN. These wells are left partially filled since they can be more effectively cleaned out just prior to processing. (Diagram courtesy of Joseph Ahadian.) 39

Figure 3-4. The plate used to hold the upper wafer. It is plexiglass, and thus transparent to the infrared light used to align the sample. Vacuum is drawn through the narrow hole drilled into the plate. This holds the sample in place during alignment. 41

Figure 3-5. Method used to flow resist into the area between the substrates. Resist is slowly added so that it fills the intersubstrate region from below, being drawn up by capillary action. This should drive out the air without trapping any bubbles. 45

Figure 3-6. This figure shows how the resist protects the surface of the target substrate. (a) shows the target substrate, with pillars bonded into wells, prior to the flowing of the resist. (b) shows the resist flowed into the area between the substrates. (c) shows the resist after baking, with bubbles rising to the top. Finally, (d) shows the source substrate removed, leaving the pillars in the wells. 45

Figure 4-1. J-V curves of wafers bonded at different temperatures. The higher temperature bond shows better linearity. 49

Figure 4-2. I-V curve for Sample 16, which was bonded at 400°C. It appears linear in the figure above, but it is not completely straight. 50

Figure 4-3. I-V curve for Sample 21, which was bonded at 500°C. It is more linear than Sample 16, shown above. 51

Figure 4-4. Profile of an unpatterned sample showing deformation. There is a noticeable depression over the area where the wafers were in contact. 52

Figure 4-5. Profile of the original, unbonded pillar on the source substrate. This plot is taken from Sample 26. 53

Figure 4-6. SEM of an unbonded pillar, wet-etched with 5:1:1 H_2O:H_3PO_4:H_2O_2. This is taken from Sample 26, and shows a pillar similar to that profiled in the previous figure. 54

Figure 4-7. SEM of an unbonded pillar, from the substrate used in Samples 29 and 30. The structure is similar to that shown in the previous figures, except that it was made by reactive-ion etching. 54

Figure 4-8. Profile of the source substrate for a deformed pillar which did not bond. This is taken

from Sample 23. 55

Figure 4-9. SEM image, with a 52° tilt, of a pillar which did not bond. It is similar to the profile shown in the previous figure, but it is taken from Sample 34. 55

Figure 4-10. Profile of the depression left by a pillar, which did not bond, on the target substrate. This is taken from Sample 23. 56

Figure 4-11. SEM image of the depression left by an unbonded pillar. It is similar to the depression in the profile in the previous figure, but it is taken from Sample 35. 56

Figure 4-12. Profile of the portion left on the source substrate by a pillar which bonded and was subsequently etched off. This is from Sample 35. 57

Figure 4-13. SEM image, with a 52° tilt, of the portion left on the source substrate by a pillar which was transferred. It is similar to the image shown in the previous profile, taken from Sample 34. 57

Figure 4-14. This shows what a pillar looks like once it has been bonded to a new substrate and etched off the original. Note the depression and the concave top. This is the target substrate for Sample 35. 58

Figure 4-15. SEM image of a transferred pillar, similar to that shown in the profile above. This is taken from Sample 34. 58

Figure 4-16. Image from an optical microscope with Nomarski interference. It shows slip lines in the source substrate of Sample 28. Note that they are oriented along the crystallographic planes, even though the pillars are at a 45° angle with it. 59

Figure 4-17. Photograph of an image from an optical microscope with Nomarski interference showing slip lines in the target substrate of Sample 28. 60

Figure 4-18. J-V curve for patterned samples. Note that the curves for Samples 28 and 30 are very similar, even though 28 was wet etched and 30 was etched by reactive-ion etching. Sample 27 was wet-etched as well. 61

Figure 4-19. Combined J-V curves for patterned and unpatterned samples. Samples 27 and 28 were patterned, while Samples 16, 20, 21, and 22 were not. 63

Figure 4-20. Resistance-area versus voltage for all samples. Samples 16, 20, 21, 27, and 28 are shown, representing patterned (27 and above) and unpatterned (21 and below) samples bonded at 400, 450, 500, and 625°C. They all originated from the same p-GaAs wafer. 64

Figure 4-21. Optical microscope photograph of the source substrate from Sample 41, which failed to bond to the OPTOCHIP. The letters GMU (marking George Mason University's portion of the chip) are clearly legible on the surface of this pillar. 65

Figure 4-22. Optical microscope photograph of the OPTOCHIP which was the target substrate for Sample 41. The letters GMU indicate where the pillar contacted the surface, missing the well it was intended for. 66

Figure 4-23. Optical microscope photograph of the source substrate for Sample 42. It shows impressions left by the OPTOCHIP's features. 67

Figure 4-24. Optical microscope photograph of the wells in which pillars failed to bond, from Sample 42. The darkened areas in the upper right corner indicate the area where the pillars were. There is also a V-shaped fragment of material in the well on the right which is reflected on the pillar. 68

Figure 4-25. Optical microscope photograph of the pillar which was in the well on the right in the previous figure. It shows a V-shaped reflection of the fragment in the well. 68

Figure 4-26. SEM image of a pillar successfully bonded into a well from Sample 43. It is flush with the side of the well. The tilt of this sample is 45^{o}..... 70

Figure 4-27. Dektak profile of the pillar in the previous figure. The sloping of the sidewalls is partially due to the limited resolution of the profiler. The walls of the pillar itself do not appear to be sloped in other observations, although those of the well are. 70

Figure 4-28. SEM image of cracks in the SiO_2 apparently stemming from some of the wells in the OPTOCHIP. These may have been caused by slip. 71

Figure 5-1. LED as grown into an OEIC well. (Courtesy of Joe Ahadian.) 76

Chapter 1

Introduction

1.1 The OPTOCHIP project

The purpose of the OPTOCHIP project is to create optical devices on commercially fabricated electronics. The electronics portion of the chip is processed out-of-house by Vitesse, leaving wells open for the devices, Light Emitting Diodes (LEDs), Vertical Cavity Surface Emitting Lasers (VCSELs), Quantum Well Innersubband Photodetectors (QWIPs), or whatever else may be required. Previous work has successfully produced LEDs inside of these wells by molecular beam epitaxy (MBE) growth. VCSELs, however, are more challenging, requiring higher quality growth than the LEDs. Wafer bonding offers an alternative method of integration. Lasers can be grown in bulk on a separate substrate, then processed into pillars to fit inside the wells. The pillars may then be bonded into the wells and separated from the original substrate.

The chief advantage of wafer bonding, aside from allowing novel fabrication techniques, is the confinement of defects. While it is possible to grow one semiconductor material on top of another, the difference in the lattice constant of the two materials places stress on them. The top layer, if grown too thick, will eventually break down, causing a defect that propagates straight through the material. This limits the thickness which can be grown, especially for materials with significantly different interatomic distances, such as GaAs and InP. The strain may affect the properties of the material as well. Wafer bonding eliminates this problem. There are still defects when two materials are bonded together, but these are limited to the interface and do not propagate very far into the body of the material.[2] This allows the integration of materials which would not otherwise be possible.

While wafer bonding has been explored as a technique for integration for some time, the

OPTOCHIP project requires something which has not been done before in III-V materials: alignment of the two chips prior to fusion. The sample patterned with pillars is simply GaAs. It is bonded to the OPTOCHIP, which has a GaAs substrate patterned with VLSI circuitry. The pillars must be aligned with the wells before the wafers are placed together and bonded. Afterward, the substrate to which the pillars were originally attached is removed. This project demonstrates that this alignment is possible under an infrared mask aligner.

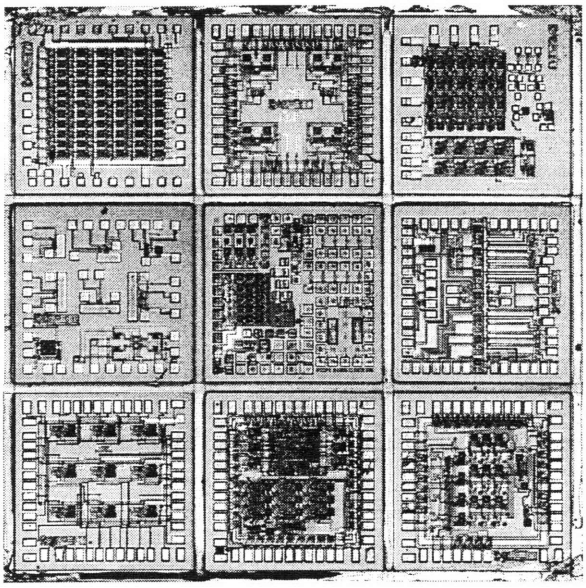

Figure 1-1. The chip created by the OPTOCHIP foundry. The chip is made up of nine patterns created by different groups. They consist of electronic circuits and wells into which optical devices are grown. In this project, the possibility of bonding devices into the wells is explored. (Photograph courtesy of Joseph Ahadian)

1.2 Thesis Outline

There are several methods of achieving wafer bonding. Chapter 2 describes a cross-section of these methods, along with their strengths and weaknesses. It also describes the mechanism of mass transport, which contributes to bonding and affects the surface morphology of the mate-

rial. Finally, dislocation motion is discussed. This is the mechanism which causes plastic deformation under pressure, and it also affects the morphology and material properties of the substrate.

The processes developed in this research are described in Chapter 3. This includes the general approach to bonding GaAs materials, followed by the methods to bond samples patterned with pillars. The chapter concludes with the procedure for aligned bonding, including the means by which the substrate that originally held the pillars is removed.

The results of the experiments, including electrical and mechanical observations, are described in Chapter 4. Chapter 5 contains the conclusions derived from the experiments, including possible directions for future research. Finally, included in Appendix II is a complete database of the experiments, recording the procedure used in each of the bonding runs and the result obtained.

Chapter 2

Wafer Bonding

2.1 Wafer bonding

Wafers are bonded together through various means. Some of the common bonding methods in use for III-V materials are epitaxial lift off (ELO), palladium bonding, and wafer fusion. Epitaxial lift off is the most flexible of these. It bonds thin films of semiconductor to various substrates. Substrates may be crystalline, such as a semiconductor, or amorphous, such as glass. This bond relies on Van der Waals force as the bonding agent, however, so it is also very weak. Palladium bonding, as its name implies, uses Pd as an intermediary between two semiconductors. While this forms a strong mechanical bond with excellent electrical properties, it is, unfortunately, quite opaque. The most attractive alternative is wafer fusion. Wafer fusion uses heat and pressure to create covalent bonds between the atoms of the two semiconductors. This gives the best optical properties, as well as excellent mechanical and electrical properties.

2.2 Epitaxial Lift Off

In Epitaxial Lift Off, a thin film of one material is transplanted onto a substrate of another material. The crucial part of this technique is the use of very thin films, which are only a few microns thick. The film is initially grown on a closely lattice-matched substrate before being etched off and transferred. The dominant bonding mechanism is van der Waals force, although hydrogen bonds, trapped charges, and other factors may come into play. Chan *et al.*[6] accomplished this method of bonding using a wax to protect the thin film sample during the etch, shown in Figure 2-1, which then provides mechanical support as it is moved to the new substrate. The

wax only needs to surround the sample, as it does in the figure, if one of the layers is vulnerable to the etchant. Otherwise, the wax is applied only at the top of the sample for the sole purpose of providing mechanical support. The bottom of the sample must be free of wax. After a DI water rinse, a film of water between the sample and the substrate allows it to be positioned. Alignment is not critical, as any alignment-dependent processing is done afterwards. Angular orientation must be done now, however. A weight is placed on top of the sample as it dries overnight. This drives the water out as it presses the two surfaces into close proximity, where van der Waals force becomes dominant. This results in a complete bond. The thinness of the film is what allows it to conform to the shape of its new substrate.

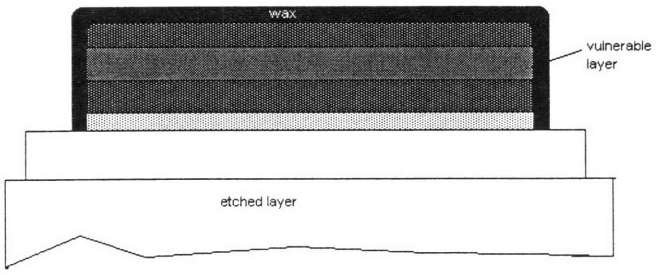

Figure 2-1. Thin film lifted off and transplanted onto new substrate. Wax protects the sides of the thin film during the etch which removes it and also provides support as it is transferred. This technique was used in the work of Chan *et al.*[6]

The main advantage of this method is its flexibility. It can theoretically be used for any type of material, as long as it has a reasonably smooth surface. AlGaAs-GaAs bonded to glass has been demonstrated.[7] The process also works at room temperature and low pressure, which allows it to be more easily integrated into semiconductor processing (since concerns of dopant diffusion or damage to metals at high temperature are eliminated).

There are, of course, disadvantages. This bond has poor electrical characteristics. It is also very weak mechanically. Van der Waals is the weakest binding force, and it does not survive the stress of processing well. Finally, the extremely thin films are difficult to handle.

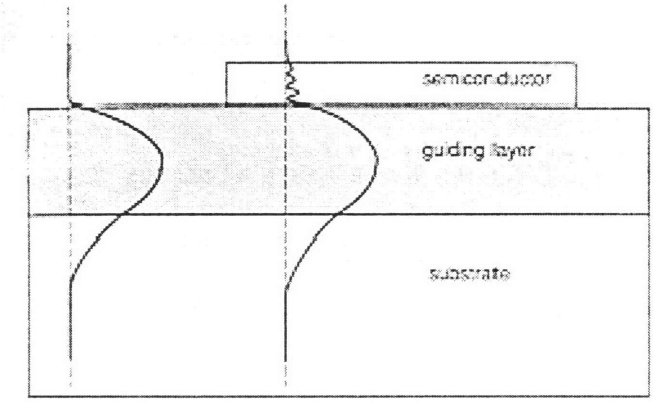

Figure 2-2. Propagation of a light-wave in the ELO bonded samples. The light coupling across the ELO bond is tested by measuring the loss in the guiding layer.[6]

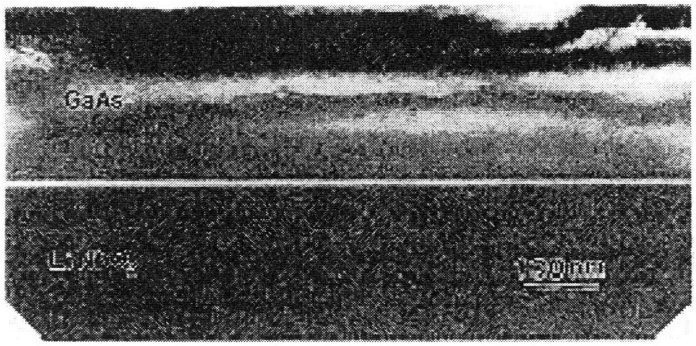

Figure 2-3. ELO bonded sample under TEM. A layer of low refractivity material, which prevents significant light coupling across the bond, is apparent.[6]

The optical characteristics observed by Chan deserve special consideration. The light coupling between a waveguide and an ELO bonded semiconductor layer (the experiment is shown

in Figure 2-2) was much lower than expected. The reason for this is believed to be a barrier layer between the two substrates with a significantly lower index of refraction. While the exact nature of this barrier was not determined (air, oxide, or some other material were suggested), the transmission electron micrograph in Figure 2-3 does show an amorphous layer between the two substrates. The thickness in the micrograph is on the order of 10 nm, but it varies over the surface. In any case, it is difficult to judge the thickness directly from the micrograph as this shows where the electron transmissivity is significantly different, and does not directly correspond to the barrier material. While this barrier decreases the coupling efficiency, it can actually be beneficial. A material with high refractive index, such as what might be used as a waveguide, placed on top of a substrate would have lower coupling losses due to this buffer layer.

2.3 Palladium bonding

Palladium bonding occurs at temperatures and pressures somewhere in between epitaxial lift off and wafer fusion. Unlike epitaxial lift off, an intermediate layer, namely palladium metal, is intentionally deposited between the wafers to be bonded. Yablonovich *et al.*[8] followed a process identical to ELO, except that the underlying substrate was first coated with palladium. Not much pressure is used, less than 15 grams per square millimeter, to drive out the water without deforming the wax. The reason for using palladium is its ability to penetrate the oxide and react with the semiconductor at temperatures as low as room temperature. It is believed that palladium forms a compound of Pd_4GaAs with the substrate. This effectively eliminates the insulating layer found in ELO, which can be seen in Figure 2-4, which shows a TEM graph of the interface from palladium bonding. Yablonovich found that a 60 nm interface layer results in a strong bond between two GaAs wafers and provides a good ohmic contact between them. Although the semiconductors may be annealed after bonding (the sample in the figure was annealed at 200°C, for example), this does not seem to significantly improve the bond.

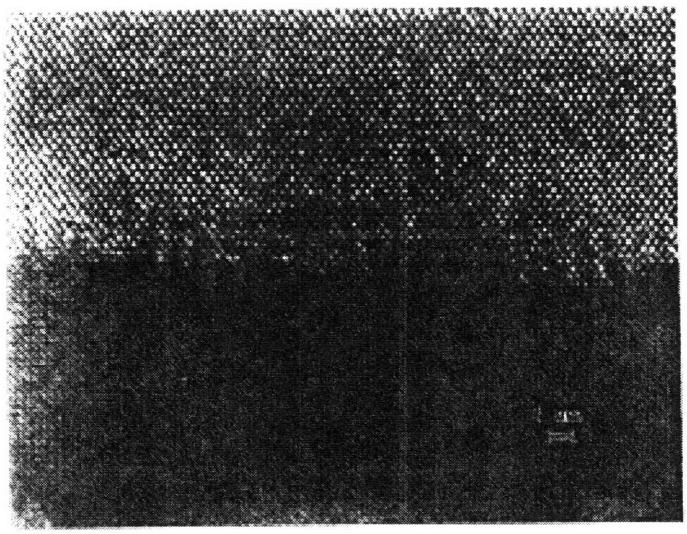

Figure 2-4. TEM of a palladium bond accomplished in a similar manner to ELO and annealed at 200°C. There is no discernible barrier layer.[8]

Tan *et al.*[9] used Pd in a wafer to wafer bonding method. They placed InP and GaAs wafers face-to-face, with Pd deposited on the GaAs, and applied uniaxial stress and heat (350°C) for 90 minutes in order to bond the samples. This type of bonding is easier to accomplish than epitaxial lift off since the wafer-sized samples are easier to handle. They found that this produced an ohmic contact between the materials, despite the difference in band gaps that would usually produce a diode-like I-V curve.

One advantage of Pd bonding is that it forms a strong bond at low temperatures and pressures. It also has excellent electrical and thermal conductivity. Pd reacts well with both elemental and compound semiconductors at low temperatures. However, the bond is ohmic, which counteracts the purpose of heterojunctions in devices. Also, the metal reflects most incident electromagnetic radiation. Tan found that a 120 nm coating of Pd on GaAs has a reflectivity of 0.8 to 0.9. A thicker coating does not further increase reflectivity. After bonding to InP, the reflectivity reduces to about 0.35 to 0.4. This reduction in reflectivity is believed to be due to the thinning of the Pd as

it bonds and the Pd-semiconductor alloy forms. Even so, this is a large reflectivity to use in optical devices, and palladium bonding is a poor choice for optoelectronic heterojunctions.

2.4 Wafer fusion

Of the technologies used to bond semiconductor wafers together, wafer fusion produces the highest quality bond. The technique was developed by Liau[1] over a decade ago. At its simplest, the semiconductor surfaces are placed in contact with one another and pressure and heat are applied to produce a strong covalent bond between them.

Liau's setup, shown in Figure 2-5, placed two wafers face to face inside a quartz tube, pressed together by a graphite fixture which fits snugly inside the tube. As the assembly was heated, graphite's higher coefficient of expansion ($9x10^{-6}$ K^{-1}, as opposed to $0.5x10^{-6}$ K^{-1} for quartz), applied strong pressure to the wafers.

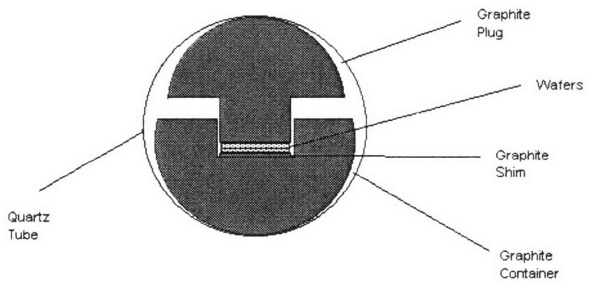

Figure 2-5. Liau's wafer fusion setup. The difference in thermal coefficients of expansion causes the graphite to expand more quickly than the quartz tube it is in. The exerts pressure on the wafers, causing them to fuse under the pressure and the heat. The graphite shim is used to get correct spacing for wafers of different thicknesses.[1]

A prominent mechanism in wafer fusion is mass-transport. When the materials decom-

pose, the Group V element forms a gas, leaving behind the Group III element. The Group V element is prevented from escaping by the wafer above it. Group III atoms are mobile (See "Mass Transport" on page 26.), and diffuse to fill in the gaps between the wafers. Since the Group V gas is trapped in the space between the surfaces, it rejoins the Group III element as the interface cools down, reproducing the crystal structure. When two different compounds are fused, the reaction during cooldown not only reforms the original compounds, but also creates an alloy of all the elements at the interface. The result is covalent bonding between the two wafers. The outcome is a strong bond which maintains the electrical and optical properties of the original wafers.

While this works well, no solution is perfect. First, this process requires high temperature and high pressure. These can wreak havoc on previous processing steps, diffusing dopants or deforming contacts and other structures. Second, the process is limited in the materials for which it is effective. Finally, since the semiconductors are not lattice matched, it is impossible to create a defect-free interface. This results in electrical traps, decreasing carrier lifetimes, and roughness at the interface, which scatters light.

The defects at the interface are an expected result of the difference in the crystal structure of the two materials. The expected linear density is:

$$\frac{4(a_1 - a_2)}{(a_1 + a_2)^2}$$

where a_1 and a_2 are the lattice constants for the two materials.[2] For InP and GaAs, this density is 5.5×10^5 cm^{-1}. An area density would be the square of this, or 3.0×10^{11} cm^{-2}. If the bond forms as expected, a per volume defect density is irrelevant, as the defects are confined to the interface and do not propagate into the surrounding material. Ram *et al.*[2] found this to be the case. No threading dislocations, which extend into the substrate, were found.

The optical properties of this bond were very good. The primary scattering for incident

light perpendicular to the interface would be the roughness of the surface. Since the surfaces are not usually atomically flat when first bonded, roughness can be expected, even though mass transport may smooth it out. Mismatched materials, however, inherently contain defects at the boundary, and Liau reports that this array of misfit dislocations produces a sinusoidal waviness in the interface.[3] Ram *et al.*[2] observed a roughness of approximately 0.4 - 0.6 nm on a bonded sample of GaAs and InP. Based on the work of Church *et al.*[4], they predicted that the total scattered light would be given by:

$$\frac{I_s}{I_i} = \frac{16\pi^2\sigma^2 R}{\lambda^2}$$

This gives the intensity of the light scattered over the intensity of the incident light. σ is the root mean square roughness, λ the wavelength of the light, and R the Fresnel reflection coefficient. This equation holds in the smooth surface limit, a nearly smooth surface perturbed by small, random roughness, such that $(2\pi\sigma/\lambda)^2 << 1$. With this equation they predicted the scattering to be $I_s/I_i = 3\text{x}10^{-8}$. It should be noted here that the roughness is not entirely random, but is believed to be periodic. Because of this, the interference which is ignored in this calculation may play a part in actual fused wafers. Still, the scattering is sufficiently small that even with this deviation significant scattering is not expected. In an interface between two identical materials, the smooth surface calculation would yield no scattering, requiring consideration of other, less prominent factors, such as the occasional voids that appear at the interface.

The electrical properties of wafer-fused bonds have been investigated both by Ram *et al.*[2] and Wada *et al.*[5] Both tested the interface between similarly doped InP and GaAs wafers. While they were uncertain of the mechanisms involved, they made several observations. First, the defects in the surface behave as traps, and Ram found that Electron Beam Induced Current (EBIC) could be used to map out defects in the material with a scanning electron microscope.

This showed recombination centers, i.e. traps due to defects, within 0.4 μm of the interface, the resolution limit of the experiment, with an average spacing of 4.6 μm. Areas further from the interface did not show these defects. Experiments with devices show that these defects do not significantly affect the device's performance if the interface is not in the active region. However, its exact effect at the barrier between the two wafers is difficult to determine. Dislocations may behave in an acceptor-like or donor-like manner, which would have different effects on the GaAs-InP heterojunction being measured. Wada focused on the I-V characteristics of the interface, and the influence of different bonding temperatures, ranging from 450-700°C. With an n-GaAs/n-InP bond, he discovered that the barrier heights of heterojunction came to 0.37, 0.4, 0.42, and 0.46 eV for samples bonded at 700, 600, 500, and 450°C respectively. The p-GaAs/p-InP I-V results, shown in Figure 2-6, were not in good agreement with his theoretical model, making it impossible to assign a barrier height for them. Wada believed that this deviation may be due to "graded carrier distributions caused by Zn diffusion, deformation of band discontinuity caused by strain, or the effect of the interface traps."[5]

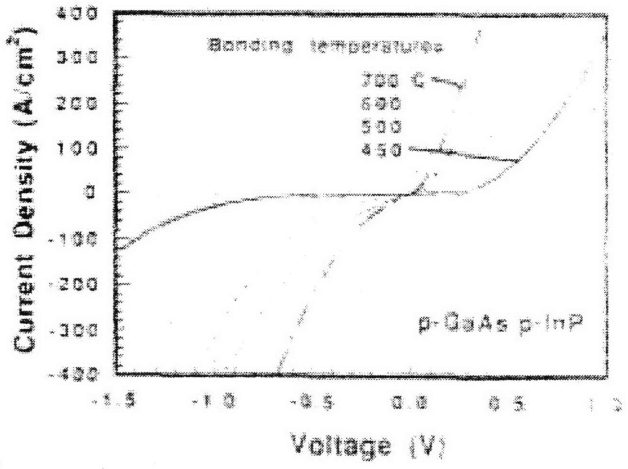

Figure 2-6. I-V curves of p-GaAs/p-InP bonded at various temperatures, as determined by Wada *et al.*[5] The structure is essentially a diode at low bonding temperatures, but becomes more linear with higher temperatures.

2.5 Mass Transport

There are numerous ways for the surface morphology of a semiconductor to change under heat and pressure. Ayabe *et al.*[10] first observed mass transport of GaAs in V-shaped grooves. The grooves would become shallow and rounded when the sample was annealed at 850°C for about an hour. This effect was noticeably dependent on time and temperature. In one variation of the experiment, an ungrooved GaAs substrate was placed face to face with a grooved substrate, separated by a small distance. This resulted in a near mirror image of the original's pattern (after being smoothed by annealing). In another variation, a 3 Torr partial pressure of AsH_3 was added. No smoothing was noticed when it was heated to 850°C for 3 hours. These results seemed to indicate that the smoothing was due to vapor-phase transport. This occurs when convex regions tend to evaporate more GaAs and concave regions tend to condense more GaAs. This occurs since the binding energy is less in convex regions, where the interatomic bonds are extended, and is greater in the concave regions, where the bonds are compressed. Liau[11] observed the same phenomenon in InP, but he believed that the limiting factor was the surface diffusion of the free indium atoms left behind when the phosphorous atoms evaporated. An ambient atmosphere of 5% PH_3 was used in the experiment to ensure that the material was not lost due to phosphorous escaping in gaseous form, leaving behind indium droplets. Free In atoms have higher concentrations at convex regions due to the same difference in binding energies which causes evaporation-condensation transport. Two other methods of mass transport are vapor-phase diffusion and volume diffusion. Volume diffusion is diffusion within the bulk of the material, due once again to the variation in chemical potential. Vapor phase diffusion combines the evaporation-condensation effect with the rate of diffusion of the vapor. Generally the vapor diffuses so quickly that vapor pressure may be considered constant. The rate at which the crystal's morphology changes is different for the various mechanisms of mass transport. Blakely[12] gives the equation

$$z_s(x, t) = z_s(x, 0)\exp\{-(AK^2 + CK^3 + BK^4)t\}$$

for the decay of the amplitude of a sinusoidal surface in time due to evaporation-condensation (A), surface diffusion (B), and volume diffusion (C), where A, B, and C are the physical coefficients associated with these factors. Note that vapor-phase diffusion is not included in this equation since it only plays a significant role when the mean free path of the atom is small compared to the wavelength of the sine wave. K is defined as $2\pi/\Lambda$, where Λ is the wavelength of the sine wave. Fourier transformation allows this equation to be used with an arbitrarily shaped surface. While all of these processes contribute, at the shorter wavelengths surface diffusion tends dominates. This would indicate that the rate of decay has a strong Λ^{-4} dependency, which Liau has observed.[13,14] However, later experiments caused Liau to revise his original conclusions, since vapor-phase diffusion of In is sometimes significant, and may show an Λ^{-4} dependency when a cover is put over the surface at a distance of $s<\Lambda/2\pi$.[15] Vapor-phase diffusion would normally tend to have a Λ^{-3} rate dependency (as opposed to the Λ^{-2} rate dependency that evaporation-condensation shows), but this does not seem to be the case here. This is due to the cover, which restricts the diffusion to two dimensions. The vapor-phase diffusion is still not the foremost consideration in InP mass transport, as the In has a small vapor pressure. However, the evaporation of In cannot be ignored, but that is more a consideration in protecting the surface from being roughened from In evaporation than for calculating the In flow.[16] The significance of vapor-phase diffusion may be different for other materials. In GaP mass transport experiments, for example, the Ga vapor pressure is more significant and may have a greater effect.

2.6 Dislocation Motion

Simple plastic flow by dislocation motion is unlikely to occur purely because of the sur-

face morphology, as only very high curvature would produce enough stress to lead to significant flow. But when stress is applied externally, such as in wafer fusion when the two wafers are pressed together, plastic deformation becomes a noticeable factor.

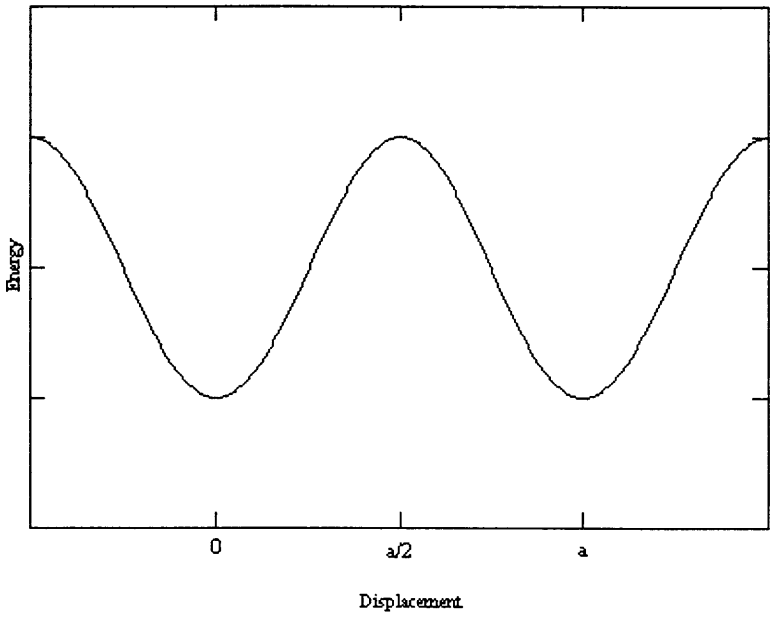

Figure 2-7. Lattice potential energy between two atoms in the crystal. It is approximated as sinusoidal. The force resisting movement is highest at a/4, where the slope is steepest. The resistance becomes very high when a whole plane of atoms must overcome a similar force.

The primary reason for deformation in crystals under stress is due to the motion of dislocations. For a perfect crystal, whose energy diagram (approximated as sinusoidal) is shown in Figure 2-7, a displaced atom will return to the minimum energy location if it is shifted by a small external force. This is an elastic motion. In order to cause an inelastic motion, the atom would need to be shifted to the next energy minimum. The force required to do that must be stronger than the highest force due to the potential energy, F=-dE/dx, which occurs at a/4. However, empirical evidence shows that the force required for plastic deformation, the yield strength, is

orders of magnitudes lower than that given by the potential energy. The reason for that is dislocations in the lattice. Consider the halfplane X in Figure 2-8(a). Note that the figure is a 2-dimensional projection of a 3-dimensional lattice. When force is applied, the crystal slips at the dislocation in a direction perpendicular to X, in effect causing X to move to the edge of the crystal, as in Figure 2-8(b). Technically, the plane itself does not move, only the defect. This causes the original halfplane to form a whole plane by joining with half of another plane, whose remaining half forms the new halfplane. This requires less stress than the previous model since the dislocation only needs to overcome one potential peak at a time. In the previous model, all the planes shifted at once, so they all needed to overcome a potential peak.

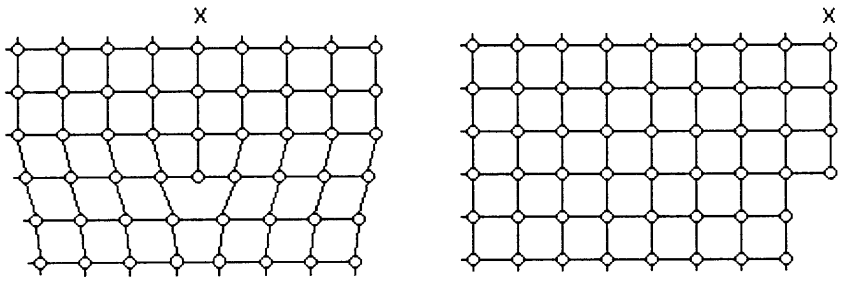

Figure 2-8. The beginning point of the halfplane dislocation is shown in (a). It can propagate through the material, one plane at a time, until it reaches (b), the end point of halfplane, at the surface of the material.

If this completely described the crystal's plastic flow, the amount of deformation readily possible would be limited to the defects already present in the crystal. This is not the case, however. Consider Figure 2-8(b). If the halfplane X is at the surface of the crystal, the step that it makes is a slip line. Slip lines are visible under an optical microscope, meaning that they must be on the micron scale. This step would have to consist of thousands of dislocations which all have

their edge on the same plane. The likelihood of all these existing beforehand is very small. Thus a mechanism for generating dislocations is necessary. If the dislocation line in Figure 2-8 is anchored at both ends by some foreign atoms, the line will not move, but it will bend. This is shown in Figure 2-9 (a and b). Line a shown in Figure 2-9 is no different from the line of defects in Figure 2-8(a). They are simply different views of the same line: one parallel to it and one perpendicular to it. The curvature of the line will not increase indefinitely, but rather the line will fold behind itself and eventually loop back until the folds intersect one another, as shown in Figure 2-9(c, d, and e) At this point a separate loop of dislocations is formed (curve f in Figure 2-9), and a new line is begun. The creation of defects effectively opens up a hole in what was once a complete plane, and then repeats the process with the next plane. This is called a Frank-Read source.[17]

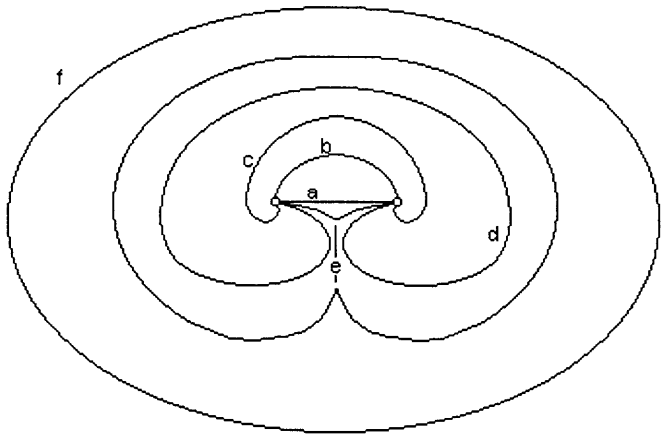

Figure 2-9. A Frank-Read source. A dislocation starts out as a straight line between two impurities which anchor it (a). This prevents the end points from moving, causing the halfplane to bend under pressure (b). Its total curvature is limited, causing it to loop back (c and d). Eventually the back loops intersect (e), creating a complete loop of dislocations (f) and a new line (a) which repeats the process.

The dislocation motion is similar, but somewhat more complex in III-V semiconductors,

which have a zincblende rather than a simple cubic structure. The half plane may terminate on atoms of either species, Group III or Group V. In addition its orientation may be directed along different planes. The two different plane types are 60^{o} and 90^{o}, where the 60^{o} plane has one dangling bond and the 90^{o} plane has two dangling bonds. These dislocations may also have an effect on the electrical characteristics of a semiconductor. The line of dangling bonds acts as a one dimensional energy band, which is half filled, lying in between the conduction and valence bands of the semiconductor. This acts as a recombination trap, capturing free electrons to form a cylindrical positively charged region in n-type material, and capturing holes to form a negatively charged region in p-type semiconductors. The exact nature of this energy band depends on the orientation of the edge and the atomic species on which it terminates. There is also the possibility that the dangling electrons along the dislocation edge may form bonds with each other: this is called reconstruction. In this case, the half filled energy band becomes two energy bands, one empty and one filled. The filled state is due to the completed bonds. The empty state is due to the antiphase defect, which appears when the reconstructed bonds switch phase. This leaves an empty bond. These two bands still work as a trap, as the half-filled band did, but its characteristics are different.[18]

The velocity of dislocations in semiconductors is in general given by the equation:

$$v = v_0\left(\frac{\tau}{\tau_0}\right)^m \exp\left(-\frac{E_a}{k_B T}\right)$$

where v_0 and τ_0 are constants of velocity and stress respectively, τ is the applied stress, E_a is the activation energy, and T is the temperature. The exponential, m, generally falls between 1 and 2, but is usually about 1. In the case of GaAs, the activation energy is about 1 eV, although it varies with doping and the type of dislocation (where the lattice is broken).[19] The exponential represents a huge change with temperature, increasing by a factor of $4x10^9$ when the temperature changes

from 300 K (room temperature) to 700 K (low-end bonding temperature). The mobility of a dislocation is defined as the velocity divided by the stress. The table below shows the factor by which the dislocation mobility increases at the different bonding temperatures. This increase with temperature means that the amount by which wafer fused samples are deformed increases not only with higher pressure, but even more so with higher temperature

Temperature (Celsius)	Temperature (Kelvin)	Mobility/Mobility at room temperature
400	673	2.0×10^{9}
450	723	6.7×10^{9}
625	898	1.5×10^{11}
800	1073	1.3×10^{12}

Table 2-1: Dislocation mobility as it varies with temperature. The temperatures given are typical bonding temperatures.

Chapter 3

Experimental Setup

3.1 The Furnace

The furnace setup which is used in this experiment was originally designed for high-purity liquid phase epitaxy. The setup was modified to hold the boat for wafer fusion, removing the graphite assembly used for epitaxy. This allows the graphite boat designed bonding to be used inside the 1.5 inch inner diameter quartz tube. The sample is heated by the furnace while in an ambient atmosphere of hydrogen inside this tube. The gas is flowed through the tube by the apparatus in the diagram in Figure 3-1. The hydrogen is purified by a Resource Systems Model RSD-2-VCR Hydrogen Purifier. This purifier passes hydrogen through a palladium barrier, which only permits hydrogen and its isotopes to pass through. The nitrogen is purified by several Matheson filters. There is also a vacuum pump, which may be used to evacuate the tube prior to starting the hydrogen flow. This was only done in the early stages of the experiment. After flowing through the tube, the gas passes through a bubbler to the exhaust tubing. Two K-type thermocouples monitor the furnace temperature, one in direct contact with the furnace and one in contact with the sample's boat. The one in direct contact with the furnace is the one used by the temperature controller. These are generally in close agreement. Figure 3-2 shows the profile of the furnace, showing the set temperature, the boat temperature (T1), and the furnace temperature (T2). The furnace was not cooled, so the ramp down rate was very slow, taking significantly longer than the rate it was set to ramp down. The controller allows programming of 8 temperature steps and the 7 intermediate times, with temperatures of up to 1020^{o}C. However, the temperature was never set above 800^{o}C.

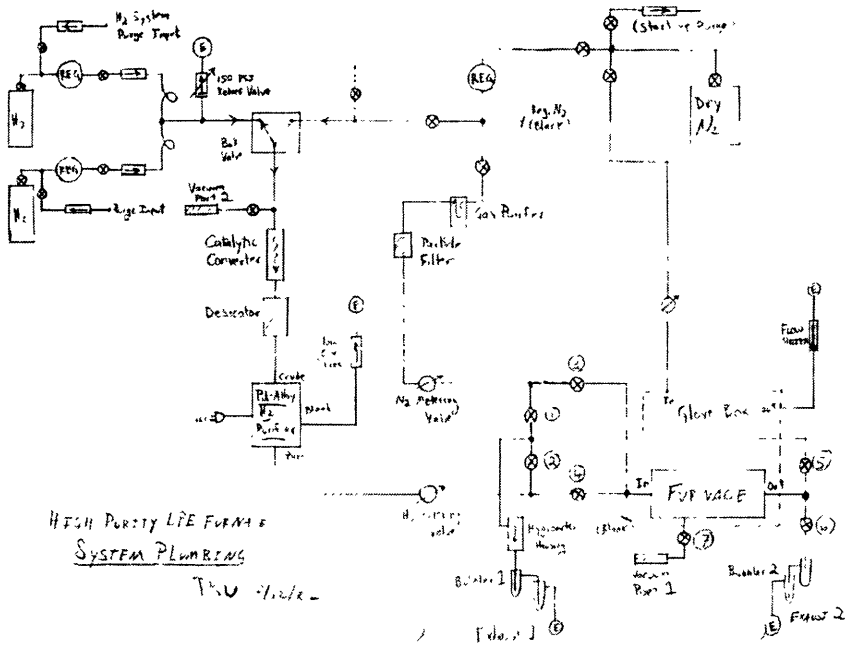

Figure 3-1. Diagram of the furnace plumbing. It shows the flow of N_2 and H_2 gases within the system. (From the LPE manual written by Peter Whitney.)

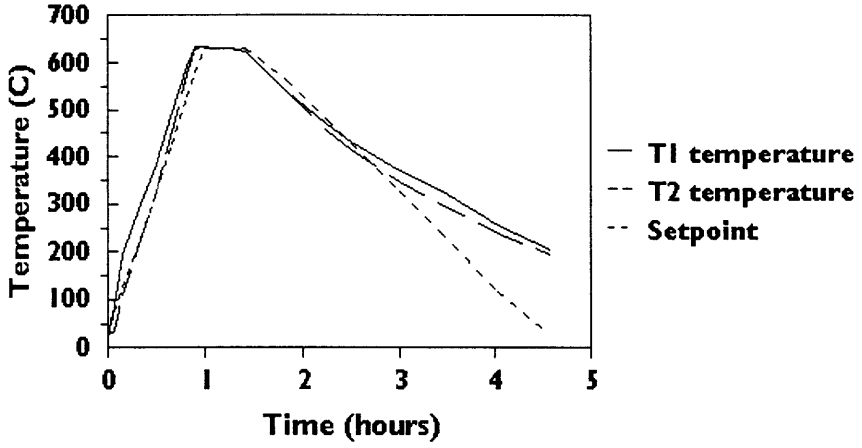

Figure 3-2. Furnace profile for a 625°C bonding run. Both the boat temperature (T1), and the furnace temperature (T2), show good agreement with the set temperature, except near the end where the exponential decay of the temperature is slower than the linear ramp rate.

3.2 Unpatterned Samples

GaAs samples were bonded in these experiments. In the initial runs, unpatterned chips of p-GaAs ranging in size from 6 mm^2 to 20 mm^2 were bonded. The surfaces of these wafers were initially coated with SiO_2 to prevent damage to the sample. The coating was etched away just prior to bonding.

The process involved in the bonding is relatively simple. Though the process was varied for the runs, the general procedure remained consistent. The exact process used in each run is recorded in the Bonding Database in Appendix II. The first step is to cleave appropriately sized samples for bonding. The cleaved samples should be square, to facilitate orientation of the crystallographic planes. The cleaning preparation for bonding begins with a full ultrasound solvent clean: this involves 5 minutes in 1,1,1-trichloroethane (or trichloroethylene), followed by 5 minutes in acetone, and finally 5 minutes in methanol. The samples are then rinsed with isopropanol and blow-dried with nitrogen. The next step is an etch. GaAs samples are simply etched in ammonium hydroxide for 2 minutes, removing any oxide, then directly transferred to a methanol bath. Samples with SiO_2 are usually etched in 4:1 H_2O:HF to remove the oxide, then placed in the methanol bath as well. Originally a 7:1 NH_4F:HF buffered oxide etch was used to remove the SiO_2, but this was found to leave an ammonium silicon fluoride residue, probably $(NH_4)_2SiF_6$, as observed by Ljungberg *et al.*[20] The purpose for using a methanol bath is to minimize any chance of forming an oxide, which would happen in air or in water. While in methanol, the samples are placed face to face. This must be done carefully, as the samples will tend to repel each other initially. Pressing down gently with tweezers will overcome the repulsion and cause the attractive forces to take over. The samples must also be carefully oriented so that they are of the same crystal orientation. As GaAs cleaves along the [100] plane, this is relatively easy to achieve as long as the edges line up. The samples are then removed from the methanol (preferably on a carrier, rather than being lifted out directly, which tends to disturb the orientation), and then placed in a

graphite boat designed to apply pressure to the sample. The boat is a proprietary design contributed by Professor Rajeev Ram. It applies pressure by graphite screws. By measuring the torque on the screws, the force, and thus the pressure, can be calculated.

The pressure applied by the assembly can, and has, been varied in order to test its effect on the sample. In general, the pressure has varied from 50 to 1000 kg/cm^2. The assembly is placed in the furnace described above, which provides the heat. The recipe for the furnace operation has also been varied, but the final recipe settled on is as follows: first the furnace is purged with nitrogen for half an hour before applying any heat. With the nitrogen still flowing, the furnace is ramped up to the baking temperature over the course of an hour. When it is at the baking temperature, the gas is switched to hydrogen, and a bake of half an hour follows. The gas is then returned to nitrogen while the furnace ramps down. Ramp down time is fairly long. This is due to the furnace itself, which, even when completely unplugged, takes a long time to cool. Nitrogen is kept flowing for the first three hours, then turned off. The furnace is usually allowed to cool overnight before the sample is removed. Baking temperatures have been varied in the course of the experiments, with the lowest being 400 and the highest being 800°C.

After bonding, the samples were tested. The next chapter describes the testing procedure and the results.

3.3 Patterned Samples

Once the process was established for unpatterned wafers, patterned wafers were used in the same process. Again, the substrates were p-GaAs. The pattern used consists of a series of square boxes ranging from 10 to 125 μm a side, applied to the samples via photolithography. The first group of patterned wafers (Samples 23-26) were wet etched with a 5:1:1 H_2O:H_3PO_4:H_2O_2 GaAs etch. This was a fast wet etch with a rate of approximately 1.5 μm/min. Later, the much slower wet etch of 10:1:1 H_2O:H_3PO_4:H_2O_2 was used, which had a rate of approximately 0.3 μm/

min. This was used for Samples 27 and 28.

These patterned samples are etched in NH_4OH just prior to bonding, to remove any oxide which formed on the GaAs. They are bonded to flat, unpatterned wafers, which undergo a similar etch: dilute HF for samples coated with SiO_2, NH_4OH for samples which were not coated. Like the previous flat wafer bonding, the source and target substrates are placed face-to-face in methanol and transferred to the furnace. (In this context, source refers to the wafer with patterned pillars. This definition will be adhered to throughout this work. Target refers to the unpatterned substrate, although the term will later refer to a wafer with wells for the pillars.) The baking step is identical to that for the flat wafers, although a smaller force is used to counteract the smaller area and to prevent the pressure from being too great.

At this point, the project shifted to the next phase, which required the transfer of pillars. Previously, the runs were simply used to test the feasibility of bonding pillars on a flat substrate. The next step was to bond the pillars and then remove the original substrate. In this case, the original substrate for the pillars is removed by a sacrificial etch of an intermediate layer. The samples used for this step were MBE grown on a p-GaAs substrate, with a 2000 Å sacrificial AlAs layer, followed by a 6 μm p-GaAs layer, which makes up the body of the pillar. These growths were unfortunately marred by gallium spitting. This left small droplets of gallium on the surface of the substrate, which in turn made bonding more difficult, both through its roughening of the surface and the excess Ga. Nevertheless, experiments were done using these samples, which have to be patterned and RIE etched, in order to etch the GaAs without etching through the sacrificial layer. A Plasma-Therm 700D Waf'r Batch Plasma Processing System is used for all PECVD and RIE steps. Prior to the photolithography, SiO_2 is deposited by PECVD as a mask for the RIE. A flow of 800 ccm NO and 900 ccm SiH_4 are deposited at a power of 20 W and a pressure of 900 mT on the substrate, which is heated to 250°C. This has a deposition rate of approximately 400 Å/min. This is then patterned using photolithography and the SiO_2 is etched in BOE. Once this is accomplished, RIE using 20 ccm $SiCl_4$ and 30 ccm BCl_3 at 225 W and 30 mT without heating the sub-

strate etches the pillars into the samples. This occurs at a rate of approximately 1000 Å/min. An RIE etch of 32 ccm CF_4 and 2 ccm O_2 at 100 W and 40 mT was originally used to remove the remaining SiO_2, but this was found to be insufficient to remove all the SiO_2, so a BOE or HF wet-etch is used. A short time period of less than 5 minutes is used to avoid etching through the sacrificial layer, which takes several hours to completely etch away in a 125 μm wide pillar. BOE is preferred to dilute HF in the samples with the sacrificial layer in order to avoid etching too far into it, but in some cases a quick HF etch is used.

The bonding procedure used for these samples is not significantly different from that used for the other patterned samples.

After bonding, the sample is placed in an HF etch which cuts through the AlAs. This takes about four hours due to the large size (125 μm) of some of the pillars.

3.4 Aligned Bonding

The steps so far, unpatterned and patterned wafer bonding, lead up to the final phase of this project, aligned wafer bonding. Once pillar transfer has been demonstrated, it is merely a matter of aligning the pillars with wells.

The wells in this case are those of the OPTOCHIP. This chip has wells designed for epitaxy-on-electronics. They are not initially clean, having layers, from top to bottom, of SiO_2, Al, SiO_2, and SiN, all above the n^+-GaAs at the bottom of the well, as shown in Figure 3-3. These are cleaned out by successive photolithography and etch steps meant to clean out the wells without damaging the rest of the chip, which has SiO_2 protecting the metal. To perform this photolithography, the darkfield OC-WC (OPTOCHIP well clean) mask is used in conjunction with a thick positive resist, SC1827, which has a spun thickness of 3 μm. This thickness is necessary to cover the uneven OPTOCHIP, and offers better protection from the etch used to remove the SiO_2. Three or four 20 minute 7:1 BOE etches are used to remove the SiO_2 above the Al, followed by a 10

minute HCl etch to remove the Al. Another three or four 20 minute BOE etches remove the remaining SiO_2 and SiN from the well. Between each etch step the photoresist, which is damaged by the etch, must be removed, and a new photolithography step must be done.

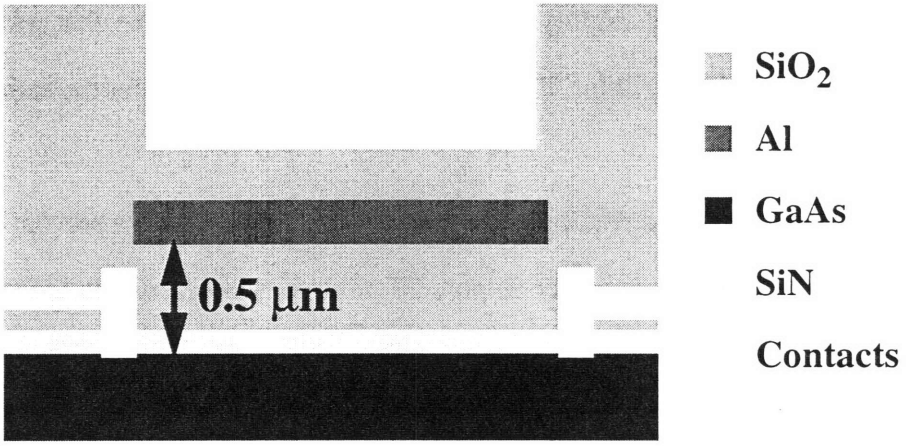

Figure 3-3. Wells in the OPTOCHIP, prior to cleaning. A top layer of SiO_2 must be removed, followed by a layer of Al, more SiO_2, and finally SiN. These wells are left partially filled since they can be more effectively cleaned out just prior to processing. (Diagram courtesy of Joseph Ahadian.)

The source substrate is a simple n-GaAs chip on which the pillars are etched by RIE. First is a PECVD step which deposits 1 μm of SiO_2 on the substrate, using the same PECVD recipe used in the previous experiments with pillars bonded to flat surfaces. The SiO_2 is then patterned using the mask PILLAR, a clear-field mirror image of the well-clean mask with slightly smaller features (recessed 5 microns from each side) and no alignment marks. This, in conjunction with Microposit S1813 positive resist, which is thinner than the SC1827, creates pillars of appropriate size for each of the wells, recessed a total of 8 μm from every side. The mirror image is necessary since the source substrate is aligned face up with the face down target substrate. It is very important that the patterning be perfect, since any obstructions to the RIE etch may result in features which will not match the wells in the OPTOCHIP, and therefore will make it impossible to place

the pillars within the wells. The greatest difficulty is at the edges, where the edge-bead removal may still leave thick, difficult to remove resist. The method used to eliminate this resist is painstaking--carefully exposing the resist with a microscope set on the highest illumination setting and high magnification. By traveling along the edges of the chip with this beam, the edges are exposed and removed in the developer. Even with the careful removal of the edge resist, the patterned sample is designed to be slightly bigger than the OPTOCHIP, so that protrusions at the edges will avoid contact with the chip. This also makes it easier to transfer the sample after alignment.

The samples are prepared similarly to the previous samples, with a solvent clean followed by an etch. The source substrate is etched in pure HF for two minutes, which thoroughly removes the SiO_2. The target substrate is etched in BOE for 5 s. This is the same preparation used immediately prior to growth for the OPTOCHIP samples on which optical devices are grown. The short time period is necessary to avoid damage to the OPTOCHIP. The samples are rinsed in methanol afterwards.

Alignment requires infrared illumination of both samples, and controlled motion of the sample within a few microns. This was done with a Research Devices MAS-400 infrared aligner. This system allows photolithography resolution alignment. The unique aspect of this setup is the way that one substrate is held above the other in order to align them. This is done using the plate design shown in Figure 3-4. This replaces the mask holder of the system, and uses the mask vacuum to secure the substrate on the plate. The plate is made entirely of plexiglass in order to be transparent to the light source, except for a small metal tube which allows the vacuum tubing for the mask plate to be attached. The holes made in the plexiglass for the vacuum are made as small as possible, since they obscure the view of the sample and make alignment more difficult.

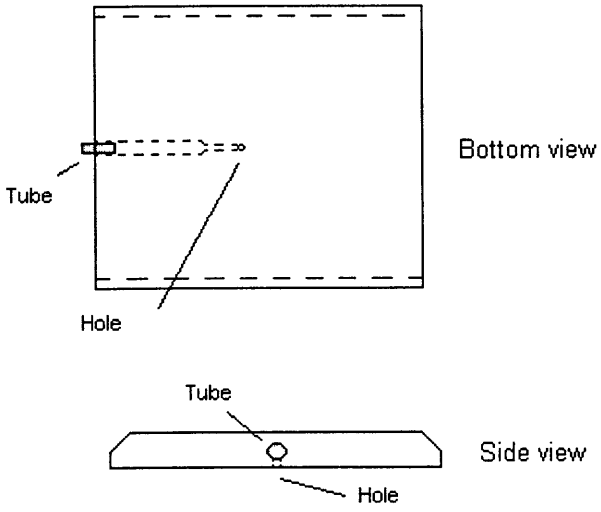

Figure 3-4. The plate used to hold the upper wafer. It is plexiglass, and thus transparent to the infrared light used to align the sample. Vacuum is drawn through the narrow hole drilled into the plate. This holds the sample in place during alignment.

Alignment itself is very similar to mask-to-wafer alignment. The OPTOCHIP is placed on the top plate, while the larger source substrate is placed below. Bringing them into proximity allows the patterns on both samples to be viewed. The reflected, rather than the transmitted, image is viewed under infrared illumination. Unfortunately, the distance needed to allow the lower substrate to move freely is large due to the uneven surface of both substrates, meaning that they are not at the same focal distance. Rough alignment at lower magnification is not difficult, but at higher magnification some manipulation of the focus is necessary to get a feel for how close the alignment is. In addition, the lower substrate is less visible than the upper substrate simply because less of the illumination reaches it, and the features of the upper substrate obscure it. It further lacks the metallic portions which help clearly define the OPTOCHIP. But while this makes the alignment challenging, it is by no means impossible. Alignment is most easily done

using the larger pillars, which may be seen more clearly. Careful manipulation of the rotation and x-y position will then bring the samples into superposition. At this point the lower substrate is slowly raised by the stage's micrometer. Careful watch will determine whether the pillar slides into place. If not, the stage may be lowered and the position of the source substrate adjusted, allowing the procedure to be repeated. Once the pillar is in position, its contact with the OPTOCHIP should allow the edges of the pillar to be clearly seen within the well. Additionally, as the pressure between the two samples increases, interference between the contacting pillar and the well, alternating dark and light as the pressure changes, clearly mark it. The stage contains a pressure sensor which measures the force of the stage against the mask, measured in kilograms. Once this force has reached 10 kg past the no-contact point the upper vacuum may be switched off. Turning the vacuum off does not necessarily release the sample. In order to ensure that the sample releases, a small amount of pressure must be applied to the vacuum tubing. While this pressure is applied the stage is slowly lowered by the micrometer, past the position where the force returns to its zero-point, until a gap between the plexiglass plate and the sample is clearly visible. Finally, the stage is lowered to its load position. The sample should not slide out of position, since the pillars are inside the wells, and that should be sufficient to hold it in place barring too rough a handling. While the OPTOCHIP did not appear to slide at all as it was moved, this supposition has not been thoroughly tested, and the sample was handled as carefully as possible. Since the larger, source substrate is on the bottom, this substrate is grasped as the sample is immediately removed from the stage and placed in the boat used for bonding. The sample's alignment can be checked again once it has been loaded into the boat. This is possible since the aligner displays the reflected image which is not blocked by the graphite. As soon as its alignment is checked, pressure is applied to the sample. This holds the two substrates in alignment as the boat is transferred to the furnace, where it is baked.

The main disadvantage to this setup is that the samples are exposed to the open air while they are aligned, allowing an oxide to form. To minimize this, they are etched immediately prior

to the alignment, and they are placed in the bonding fixture and moved to the furnace immediately afterwards. This helps minimize any oxide formation, but it does not eliminate it, especially since the alignment step is difficult and may take long enough that it neutralizes the precautions.

The bonding run ideally uses a temperature of 470°C, the highest temperature to which the OPTOCHIP can be heated without damaging the metal interconnects and contacts. This is the temperature used when devices are grown into the wells by molecular beam epitaxy. This is higher than 450°C, the lowest temperature at which bonding has been reliably demonstrated. However, to improve the quality of the bond, a temperature of 530°C was used. This causes some damage to the contacts, but it is not severe, and the electronic circuits are not damaged. To further improve the bond, the time period of the bake was increased to 3 hours, as compared to the normal half hour bake time. The pressure is approximately equivalent to 375 kg/cm^2.

Once the bonding run is complete, the source substrate needs to be removed. Originally, this was to be done by a combination of mechanical lapping and chemical etching. However, the lapping left the substrate uneven so that the chemical etching removed part of the substrate long before it removed all of it. Since there is no etch-stop, this allowed the etch to completely etch through some of the pillars before the entire substrate was removed. Therefore, the technique used was to wet etch completely through the source substrate. In order to protect the underlying OPTOCHIP, the gap between the two wafers is filled by a thin photoresist, specifically Microposit S1813, using capillary action. This is done by the method shown in Figure 3-5. The sample sits on a slanted slide in a small beaker. Resist is gradually added to the beaker to fill the inter-substrate region. It is necessary to go slowly so that no air is trapped between the substrates. Figure 3-6(a and b) shows a cross-section of the OPTOCHIP and its associated source substrate immediately after bonding and while the resist is flowed into the gap between the substrates. The sample is baked on a hotplate, which is ramped to 130°C, where the sample is left for 15 minutes. The hotplate is used, with the OPTOCHIP on the bottom, to prevent the formation of bubbles at the surface of the OPTOCHIP. Baking resist appears to evolve a gas which forms bubbles in the

resist. Heating the resist from below, however, allows the gas to rise in the as yet unbaked resist. The bubbles migrate to the top of the resist, in direct contact with the source substrate. The source substrate is about to be etched away: openings in the resist at its surface has little affect. The surface of the OPTOCHIP, however, is still protected by the thin layer of resist which remains at the bottom. This is shown in Figure 3-6(c). After baking, the sample is then placed in a wax, which protects the sides of the underlying target substrate while exposing the source substrate. Any resist on the back of the source substrate is removed by scraping it off with a razor blade and then applying acetone with a cotton swab to remove any remaining resist. The sample is etched in a fast wet etch of 8:1:1 H_2O_2:H_2SO_4:H_2O. This etchant will attack Crystal Bond, the preferred wax, but it will most certainly etch through the substrate, which it does at about 15 μm/min, before this becomes a problem. Once it has cut through most of the substrate, a slower 5:1:1 H_2O:H_3PO_4:H_2O_2 etch, which has a rate of about 1.5 μm/min, is used until the pillars are revealed. This is shown in Figure 3-6(d). The resist protects the OPTOCHIP from being damaged when the etch has broken through the source substrate. The difficulty here is due to the fact that the pillars have no etch stop. If the etch is not smooth and removes part of the substrate much more quickly than the rest, the etch will go straight through the pillar and into the substrate beneath it. A smooth etch is definitely preferred. This requires agitation of the sample in the etch, and lying the sample horizontal in the etchant. If it is vertical or slanted, due to the slide, the fast etch will tend to etch the upper part of it more quickly. If part of the substrate is etched through more quickly, resist may be moved to protect that part of the substrate from overetching. This does leave the pillar heights uneven, however. Afterwards, the resist may prove difficult to remove. NMP (1-methyl-2-pyrrolidinone), held at a temperature from 60 to 90 ^{o}C, should remove it within 20 minutes, however.

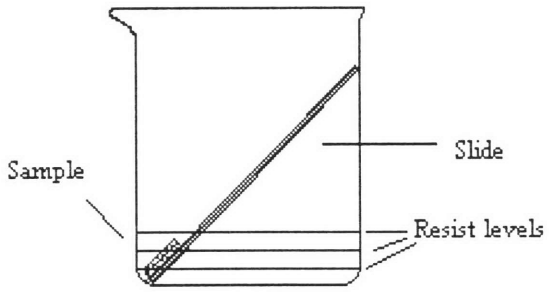

Figure 3-5. Method used to flow resist into the area between the substrates. Resist is slowly added so that it fills the intersubstrate region from below, being drawn up by capillary action. This should drive out the air without trapping any bubbles.

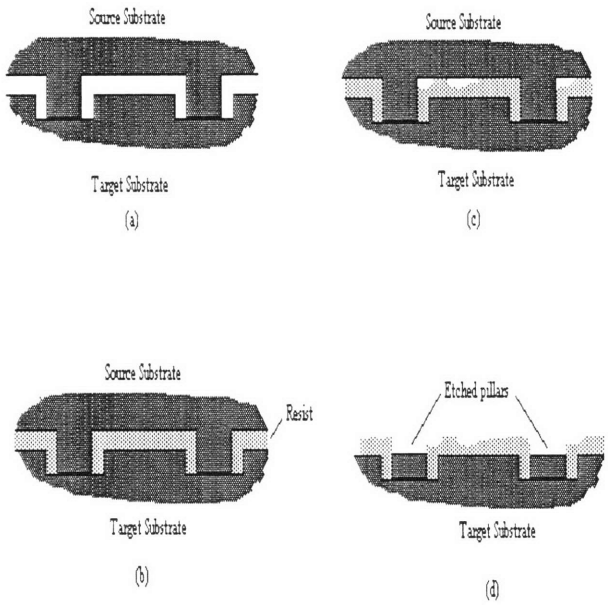

Figure 3-6. This figure shows how the resist protects the surface of the target substrate. (a) shows the target substrate, with pillars bonded into wells, prior to the flowing of the resist. (b) shows the resist flowed into the area between the substrates. (c) shows the resist after baking, with bubbles rising to the top. Finally, (d) shows the source substrate removed, leaving the pillars in the wells.

Chapter 4

Results

4.1 Unpatterned Samples

The results of the early bonding experiments indicate that higher temperatures allow for easier bonding. Temperature seems to be a more significant factor than pressure. A large pressure is necessary, but once this condition is met, even order of magnitude variations do not appear to affect the quality of the bond. Variations in temperature produce more noticeable results. While bonding is possible at temperatures as low as 400°C, it is difficult to reproduce. In fact, only one sample showed good mechanical and electrical properties at this temperature. Successful bonding is determined by the ability to cleave the bonded sample without the bond breaking. This demonstrates that the bond has nearly the strength of the crystal structure itself, preferring to break along the cleaving plane than the bond. In contrast to the low temperature bond, the bonding at higher temperatures is readily reproducible. 625°C is a reasonable temperature for bonding, and 800°C has very good reliability and strength. Unfortunately, these temperatures are inappropriate for the OPTOCHIP project, where temperatures above 470°C cause damage to contacts and dopant diffusion.

Higher temperatures are also less sensitive to roughness and particles on the surface of the samples. Bonding requires smooth surfaces, but this requirement is not as rigid as with epitaxy. Mass transport often compensates for roughness on the surface. Sensitivity to roughness was particularly noticeable on samples bonded at 450°C. The smooth, epitaxy ready samples bonded well at this temperature. Other samples, where epitaxial growth had exhibited problems with gallium spitting, did not bond This is most likely due to the roughness caused by the spitting, although the excess gallium may also be a factor. (It should be noted that these bonding runs at

450°C were carried out on patterned samples, although the effects had little to do with the patterning.)

Another factor is the electrical conductivity of the bonded wafers. One difficulty involved here is that the contacts for many of the samples were made prior to the bonding. The reason for this was twofold: first, part of the experiment was to determine if the bond could be made without harming metal already on the samples; second, it was preferred that the metal contacts be made beforehand, rather than affecting the bond afterwards. As a result, at the higher temperatures, where the best bonding occurs, the metal contacts were often damaged. At the lower temperatures, where the contacts were not damaged, the bond itself tended to be poor. The J-V (current density versus voltage) graphs below are representative of some of the results. All the curves are of bonding between two p-type GaAs samples taken from the same wafer. To the degree possible, the samples possessed the same planar orientation. The curves at 400°C are very similar to the curves observed by Wada *et al.*[5] for p-GaAs/p-InP at 450°C (compare to Figure 2-6). Different line types represent different temperatures.

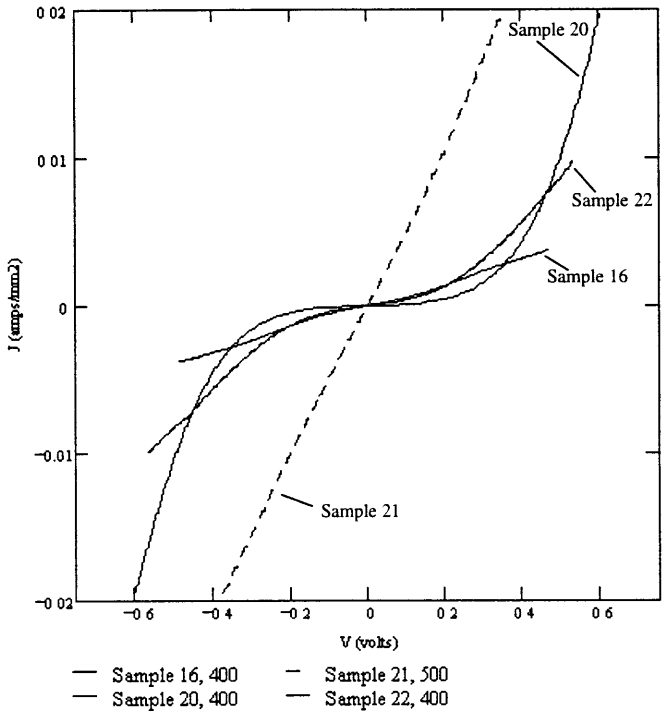

Figure 4-1. J-V curves of wafers bonded at different temperatures. The higher temperature bond shows better linearity.

Since the two samples bonded are identical materials, rather than the p-GaAs/p-InP bonding done by Wada, the ideal result is a straight line, evident of an ohmic contact. This is seen in two of the samples, one bonded at 400°C and one bonded at 500°C. Since these are difficult to determine from the above graph, the two are shown below in Figure 4-2 and Figure 4-3. Curiously, the other 400°C bonding samples showed characteristics closer to those observed by Wada at 450°C. It should be noted that the 400°C sample with the good ohmic contact is the only one to show a good mechanical bond, while the majority have poor electrical and mechanical performance. The reason why this one shows such good performance is not known, although one possibility is that the surface was cleaner or smoother when it was bonded. The curves for this sample and the 500°C sample, Samples 16 and 21, respectively, are not as straight as they appear in the

first figure, as can be seen below. The sample baked at 500°C has a more linear curve, but it is clear that the contact is not seamless even for these.

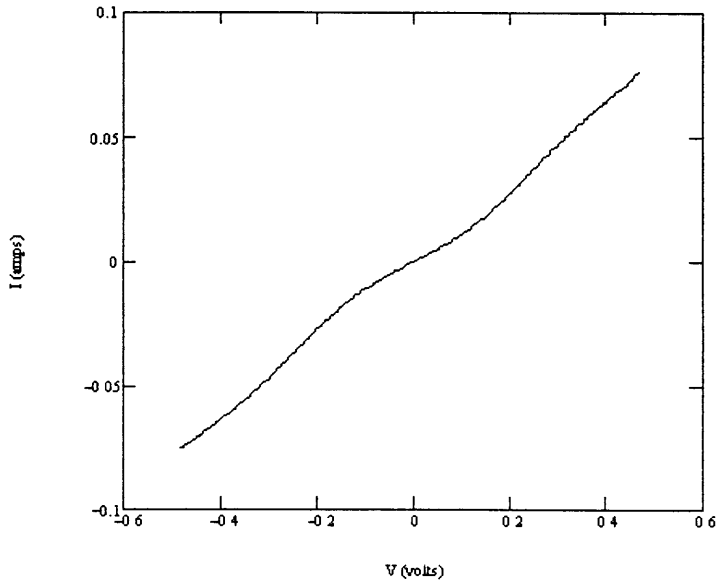

Figure 4-2. I-V curve for Sample 16, which was bonded at 400°C. It appears linear in the figure above, but it is not completely straight.

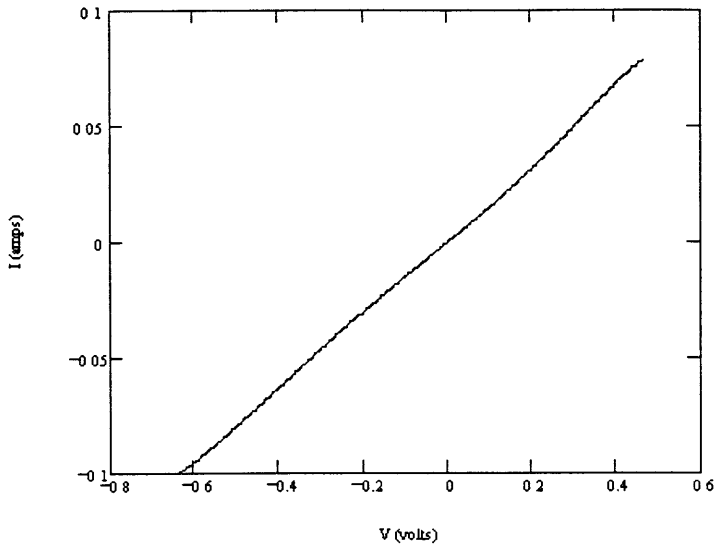

Figure 4-3. I-V curve for Sample 21, which was bonded at 500°C. It is more linear than Sample 16, shown above.

True to the principles of dislocation motion discussed in Chapter 1, the pressure and temperature applied to the substrate causes it to deform. Figure 4-4 shows the profile, measured with a Sloan Technology Dektak 8000 profiler, of a sample over an area where a bond failed to form, but where a depression was left by the force applied. The peak at one edge is of the area just outside where the two wafers were placed together. The valley is where the bond should have taken place. This appears to be the result of dislocation motion. These observations are discussed in more detail in "Pillar Bonding" on page 52.

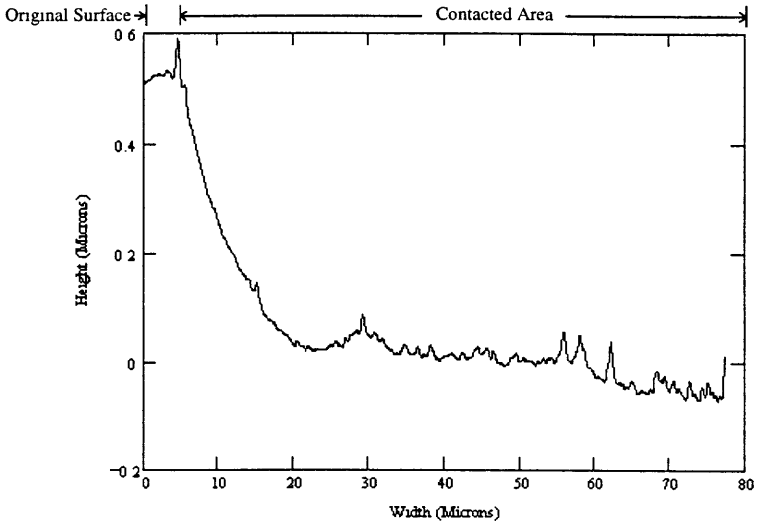

Figure 4-4. Profile of an unpatterned sample showing deformation. There is a noticeable depression over the area where the wafers were in contact.

4.2 Pillar Bonding

One of the chief difficulties in the bonding was not due to the alignment but to the structures, and the pressures, involved in the bonding. Usually, wafer bonding is done over a relatively large area, from a few square millimeters to entire wafers. In this case, however, square pillars are etched into the samples, with widths ranging from 10 μm to 125 μm. These pillars are bonded to an unpatterned wafer with a smooth surface. This causes a problem in the force applied. The equipment which applies the force is not precise enough to give a small enough force to result in a pressure similar to that used with the flat samples. The much smaller bonding area means that a much larger pressure is applied at the bonding interface, despite the fact that less force is used. This causes greater plastic deformation of the samples, resulting in sunken pillars on the source substrate and depressions in the target substrate. The following series of figures shows different

pillar bonding results in Dektak 8000 profiles, each accompanied by an SEM image of a similar pillar. The profile of the initial pillar structure, prior to the bonding experiment, is shown in Figure 4-5, and is accompanied by two SEM images, one for an RIE etched structure and one for a wet-etched structure. The profiles in Figure 4-8 and Figure 4-10 show the deformation of the source pillar and the target substrate, respectively. The source substrate appears rough due to the RIE etching, which also left the edges of the pillars ragged. This makes it difficult to see the deformation. This roughness is particularly evident in Figure 4-9. This deformation is most easily seen on samples which went through a bonding run but did not bond (primarily samples run at 400°C), especially if the substrate is smooth. Evidence also exists in good bonding, however, as shown in Figure 4-12 and Figure 4-14, which are profiles of the stump left behind by a transferred pillar and of the transferred pillar itself, respectively. The transferred pillar sits in a depression, and the top of the pillar appears to be indented to match the depression at the bottom.

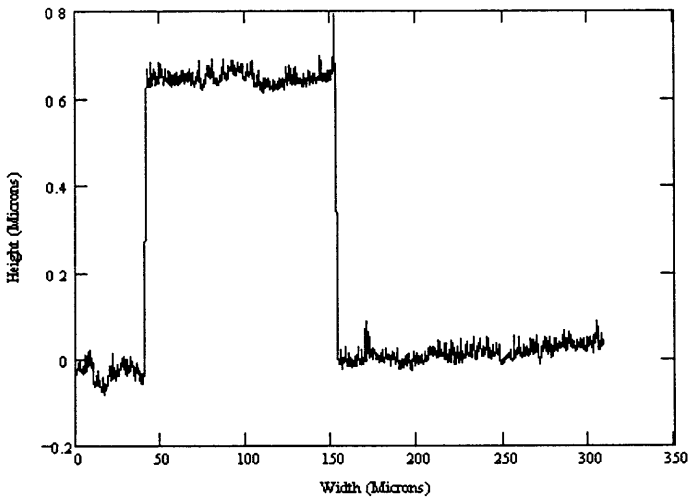

Figure 4-5. Profile of the original, unbonded pillar on the source substrate. This plot is taken from Sample 26.

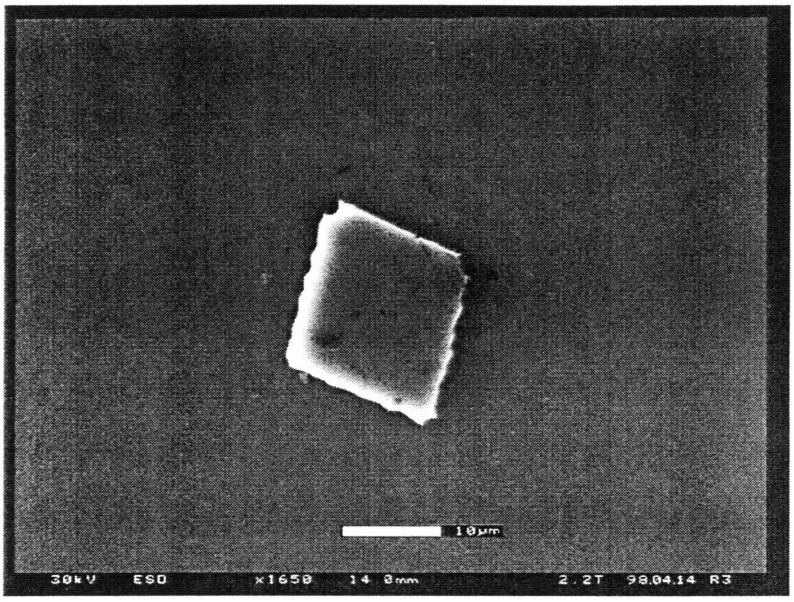

Figure 4-6. SEM of an unbonded pillar, wet-etched with 5:1:1 H_2O:H_3PO_4:H_2O_2. This is taken from Sample 26, and shows a pillar similar to that profiled in the previous figure.

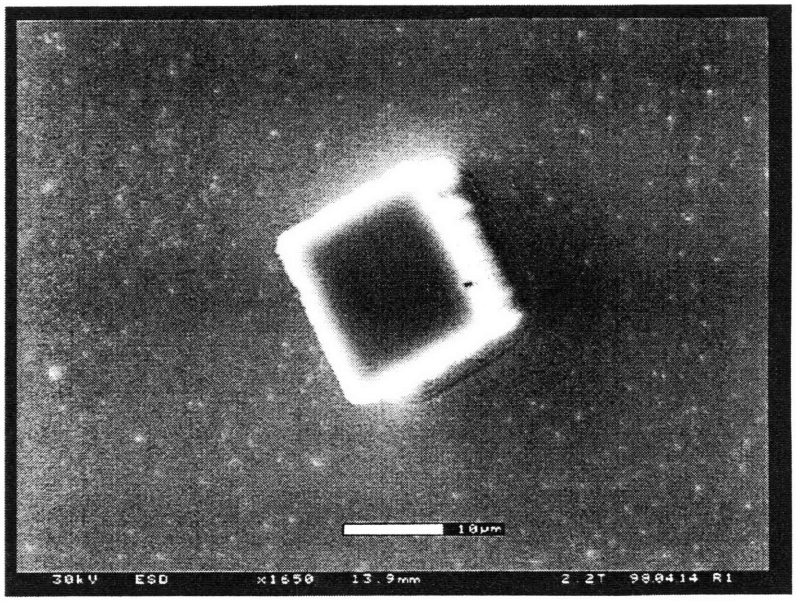

Figure 4-7. SEM of an unbonded pillar, from the substrate used in Samples 29 and 30. The structure is similar to that shown in the previous figures, except that it was made by reactive-ion etching.

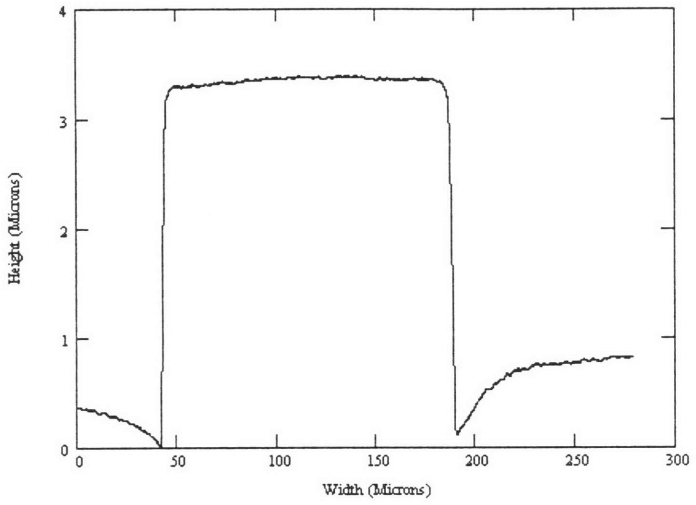

Figure 4-8. Profile of the source substrate for a deformed pillar which did not bond. This is taken from Sample 23.

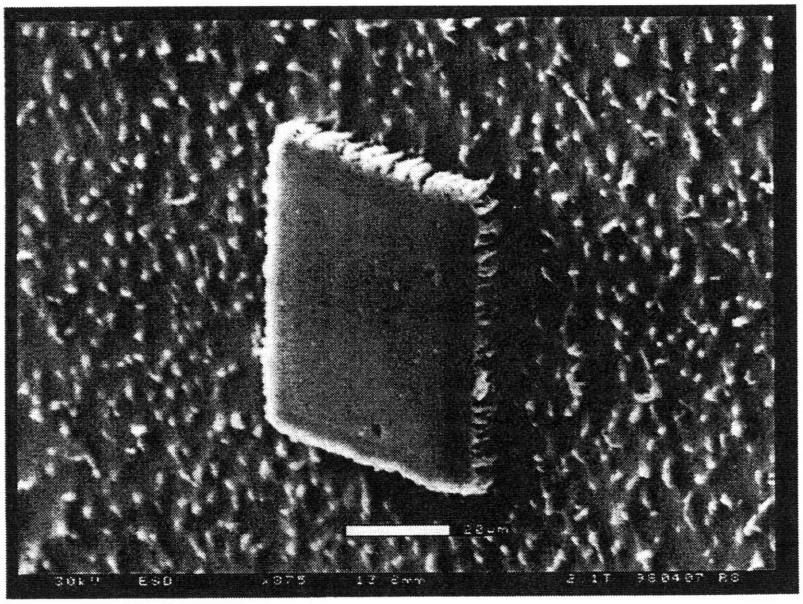

Figure 4-9. SEM image, with a 52^{o} tilt, of a pillar which did not bond. It is similar to the profile shown in the previous figure, but it is taken from Sample 34.

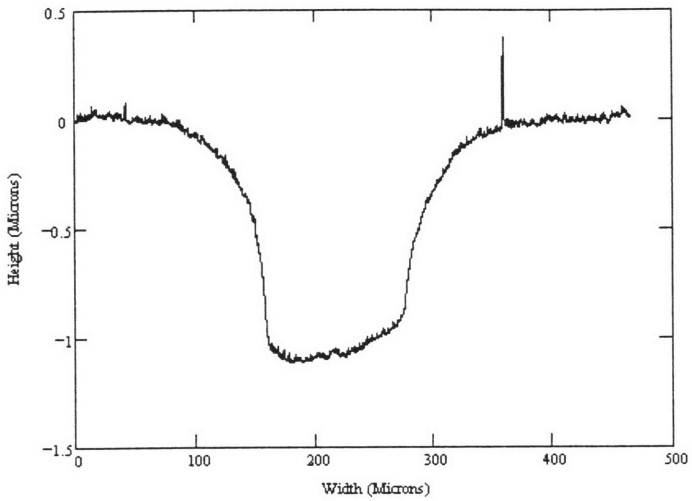

Figure 4-10. Profile of the depression left by a pillar, which did not bond, on the target substrate. This is taken from Sample 23.

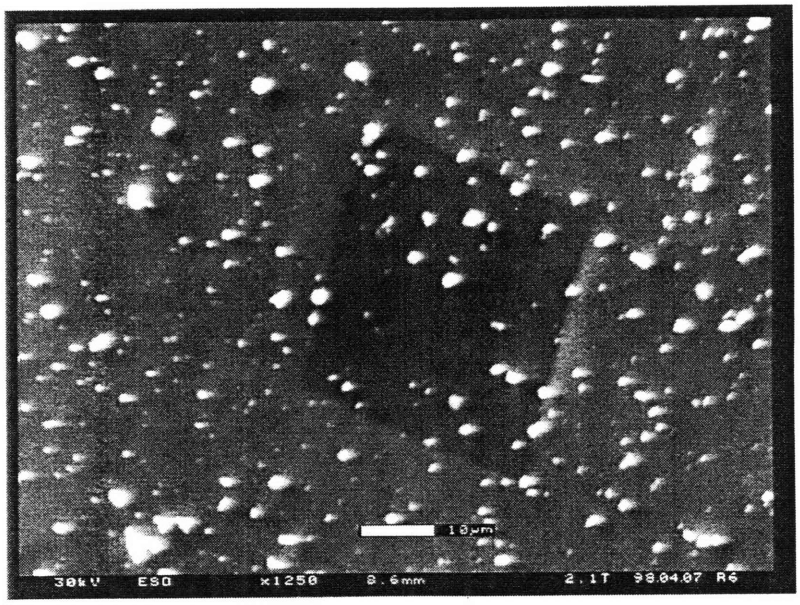

Figure 4-11. SEM image of the depression left by an unbonded pillar. It is similar to the depression in the profile in the previous figure, but it is taken from Sample 35.

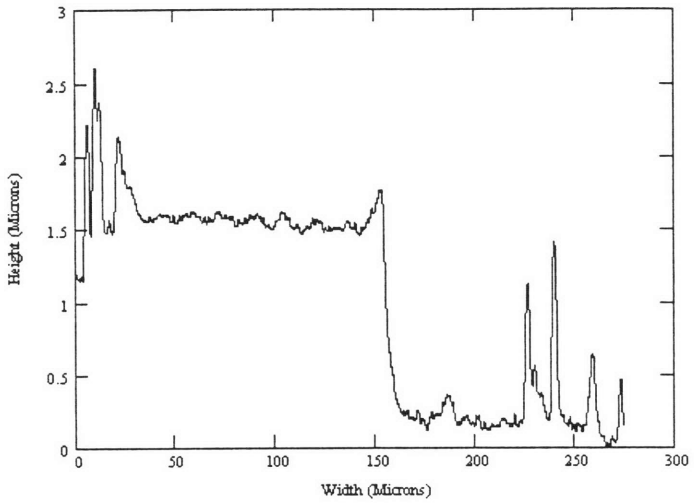

Figure 4-12. Profile of the portion left on the source substrate by a pillar which bonded and was subsequently etched off. This is from Sample 35.

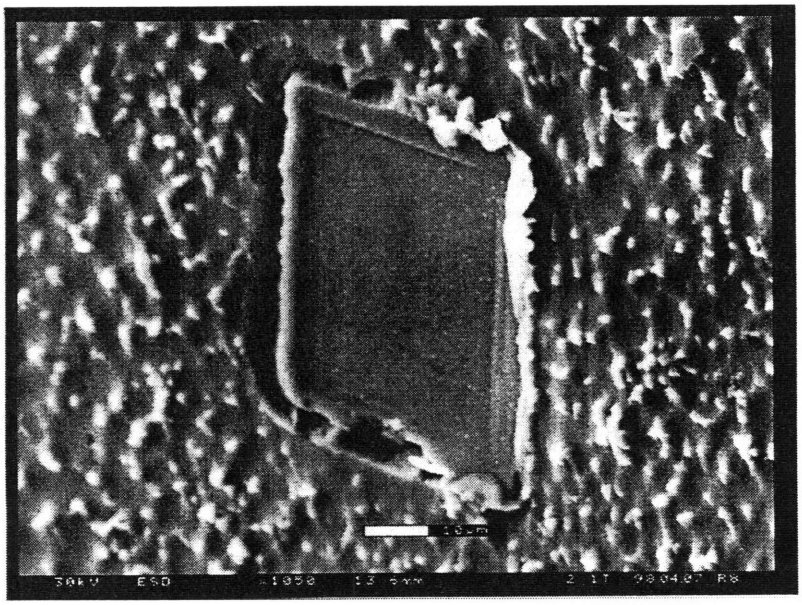

Figure 4-13. SEM image, with a 52^{o} tilt, of the portion left on the source substrate by a pillar which was transferred. It is similar to the image shown in the previous profile, taken from Sample 34.

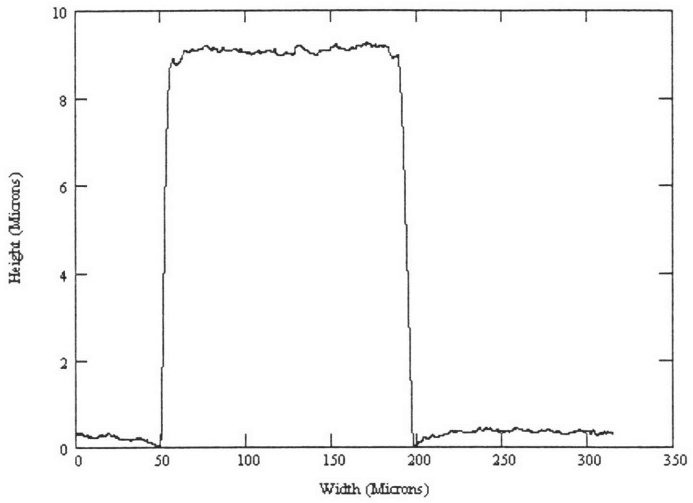

Figure 4-14. This shows what a pillar looks like once it has been bonded to a new substrate and etched off the original. Note the depression and the concave top. This is the target substrate for Sample 35.

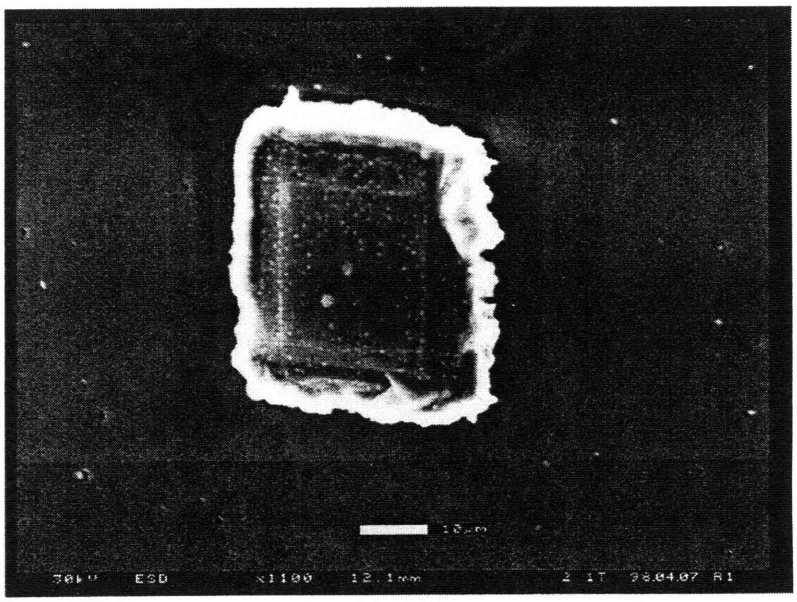

Figure 4-15. SEM image of a transferred pillar, similar to that shown in the profile above. This is taken from Sample 34.

This deformation is not due to the pressure alone, as an experiment with wafers of similar structure failed to produce any deformation, or bonding, at room temperature. And low pressure at a high temperature produces similar results, or lack of them. The pressures involved are large: approximately 300 kg/cm^2 was applied to the sample shown in Figure 4-8 and Figure 4-10. That is nearly an order of magnitude larger than the typical applied pressure. Determining the mechanism behind the deformations is fairly simple, however. Under an optical microscope, with Nomarski interference, a pattern of slip lines is clearly visible. Slip lines are created as the crystal slips along the crystallographic planes, bringing lines of defects to the surface. These lines are shown in the photographs in Figure 4-16 and Figure 4-17. These lines are along the crystallographic planes, even when the pattern is not, as in the below figures. This clearly indicates that the primary mechanism behind the deformation is dislocation motion, although the other mass transport mechanisms may affect the morphology as well.

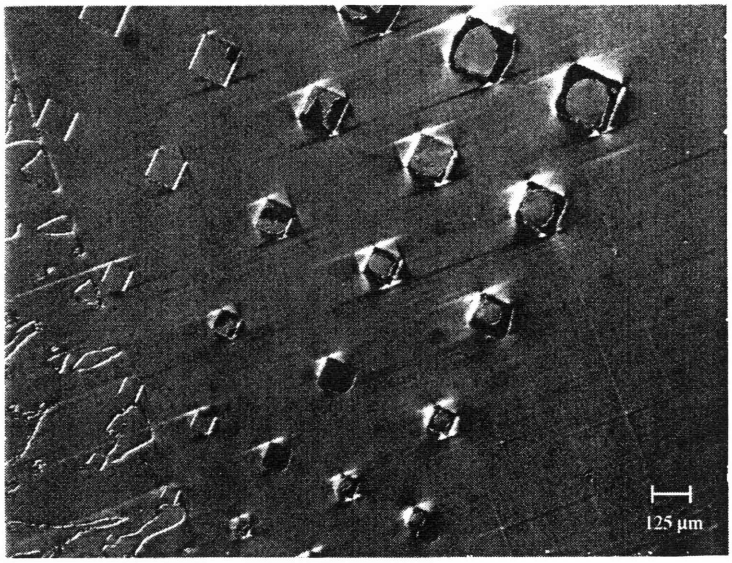

Figure 4-16. Image from an optical microscope with Nomarski interference. It shows slip lines in the source substrate of Sample 28. Note that they are oriented along the crystallographic planes, even though the pillars are at a 45^o angle with it.

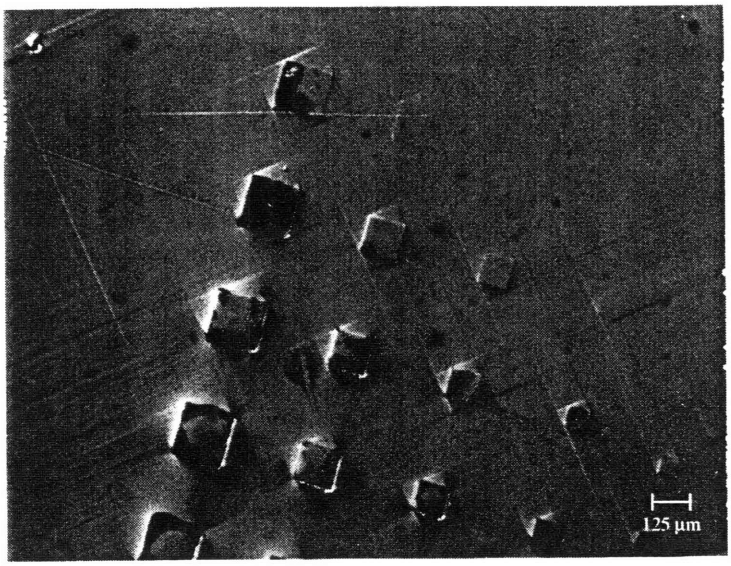

Figure 4-17. Photograph of an image from an optical microscope with Nomarski interference showing slip lines in the target substrate of Sample 28.

Shown below are the J-V characteristics observed for select pillar bonded wafers. There are a few significant attributes. First, the curve for the sample bonded at 625°C, the only sample bonded at that temperature whose contact was good enough to allow this kind of measurement, is more linear than the curves for the samples bonded at 450°C, but also has less steep of a slope, indicating a higher resistance. In addition, this sample is bonded over more than one pattern, and thus has a larger area. Reducing this area in the calculation of the current density to equal that of the other two samples brings it closer to match their J-V curve, but it still has a larger resistance. It is possible that the 625°C sample bonded over a smaller area than used in the calculations. It may also be possible that the contacts are more damaged than they appeared.

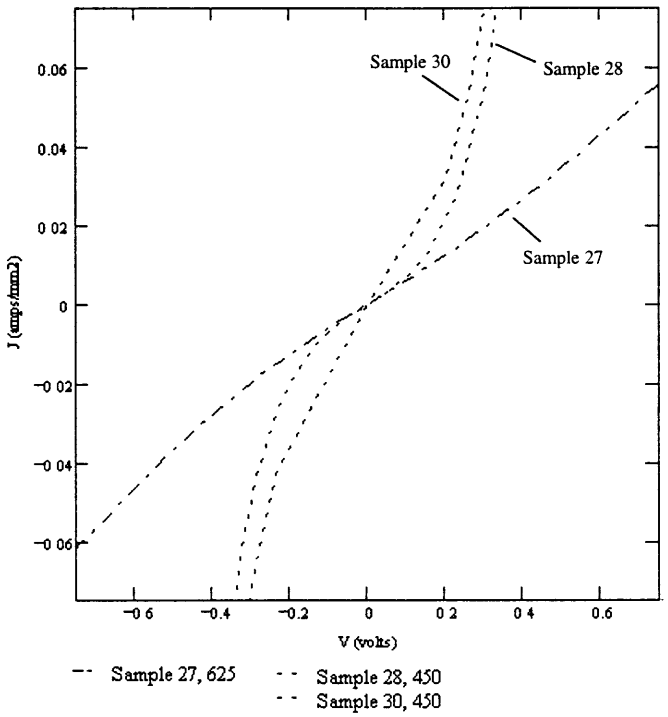

Figure 4-18. J-V curve for patterned samples. Note that the curves for Samples 28 and 30 are very similar, even though 28 was wet etched and 30 was etched by reactive-ion etching. Sample 27 was wet-etched as well.

4.3 Comparison of Electrical Characteristics of Flat and Patterned Wafers

Figure 4-19 below compares the J-V curves of the samples, both patterned and unpatterned. Since the two samples bonded at 450°C were similar, only Sample 28 is shown, and only Samples 16 and 20 are shown of the samples bonded at 400°C. All the patterned samples, no matter what temperature, had a lower resistance-area. One possible explanation derives from the process used to bond the samples. Methanol was left in between the samples when they were bonded. In the unpatterned samples, some of this methanol was very likely trapped between the samples when they were bonded, leaving non-conductive materials between the surfaces, similar

to what was seen in the ELO experiments. In the patterned wafers, the area of bonding was much smaller, and the methanol could have been more easily pressed to the edges of the bonded material and escaped through the open area between the substrates. Another factor may be errors in the calculation of the contact area. The difference in resistance between the samples bonded at 450°C and those bonded at 400°C is much smaller than the difference in resistance-area. However, the difference in resistance between the samples bonded at 500°C and 625°C is much larger than the difference in resistance-area, such that the sample bonded at 625°C has the largest resistance and that bonded at 500°C has the smallest. It may be that the contacts on the 625°C sample are damaged more than first believed, which would help to explain why the sample has a higher resistance than all the other samples, and a higher resistance-area than the two 450°C sample. This would lend credence to either the theory of wider contact area for the 450°C samples or the theory of an intermediate layer left by the methanol. The intermediate layer would be the more likely explanation. First, because similar effects were observed by Chan, and secondly, because there is no other indication that the 450°C samples bonded over a much larger area than expected.

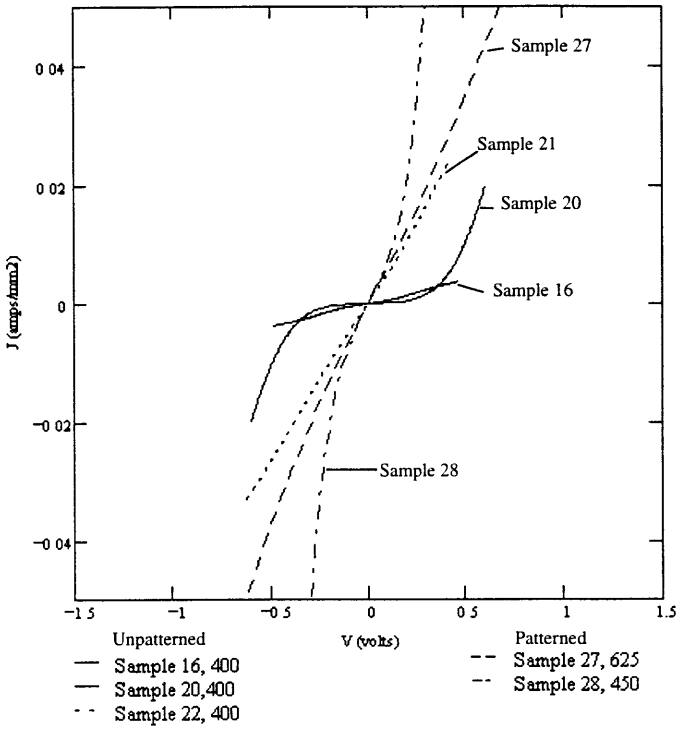

Figure 4-19. Combined J-V curves for patterned and unpatterned samples. Samples 27 and 28 were patterned, while Samples 16, 20, and 21 were not.

Figure 4-20 below shows the resistance-area of the samples as a function of voltage. This calculation is based on the inverse of the derivative of the J-V curves above. The graph is semi-logarithmic, which makes it much easier to compare some of the samples. Due to the discrete nature of the data, some of the curves are very choppy, especially that of Sample 21. In any case, it is readily apparent that Samples 21 and 27, the samples bonded at 500 and 625°C respectively, are very similar to one another in terms of resistance-area. The samples bonded at 400°C, are also rather similar in magnitude, although Sample 16 has a nearly sinusoidal curve. The sample bonded at 450°C is again the wildcard, with a much smaller resistance-area than any of the others.

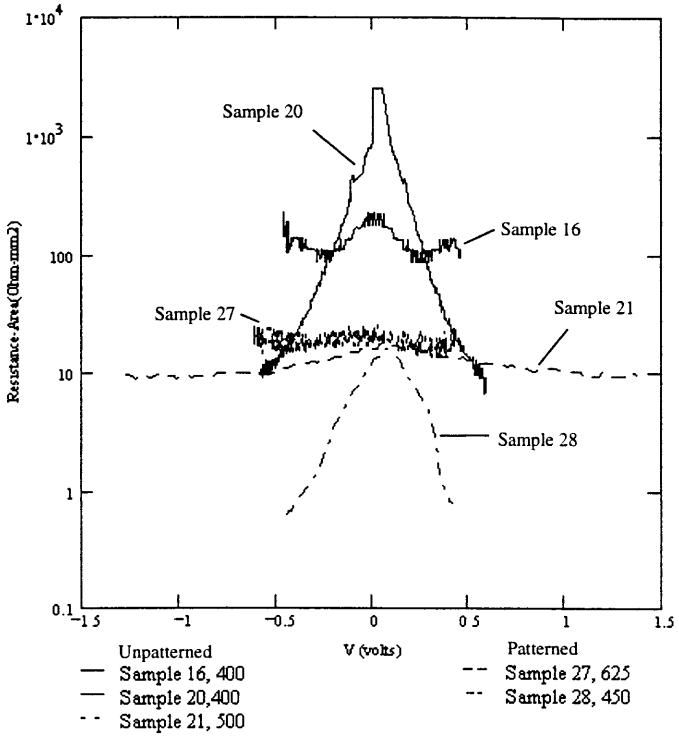

Figure 4-20. Resistance-area versus voltage for all samples. Samples 16, 20, 21, 27, and 28 are shown, representing patterned (27 and above) and unpatterned (21 and below) samples bonded at 400, 450, 500, and 625°C. They all originated from the same p-GaAs wafer.

4.4 Aligned Wafer Bonding

The final stage of the experiment required infrared alignment between the source and target substrate. The target substrate was the OPTOCHIP, with clear wells down to the GaAs substrate into which the pillars on the source substrate were bonded. The alignment procedure which presented the greatest challenge was the transporting of the sample from the aligner to the boat used in fusion. The first OPTOCHIP sample, Sample 41, did not bond simply because it was not aligned. This was due to the fact that the upper wafer, the OPTOCHIP in this case, adhered to the

plexiglass plate when the vacuum was released. This may be due to static, or the fact that turning off the vacuum which holds the chip in place still leaves the vacuum line at low pressure. The misalignment left clear impressions on the top of the source substrate pillars when they failed to bond, reflecting the features of the OPTOCHIP where they did contact. Figure 4-21 and Figure 4-22 show this, demonstrating a high degree of misalignment for Sample 41.

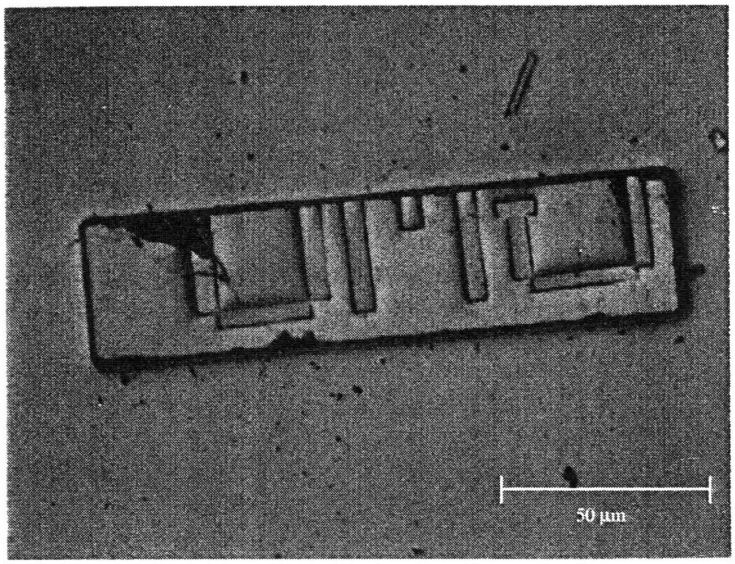

Figure 4-21. Optical microscope photograph of the source substrate from Sample 41, which failed to bond to the OPTOCHIP. The letters GMU (marking George Mason University's portion of the chip) are clearly legible on the surface of this pillar.

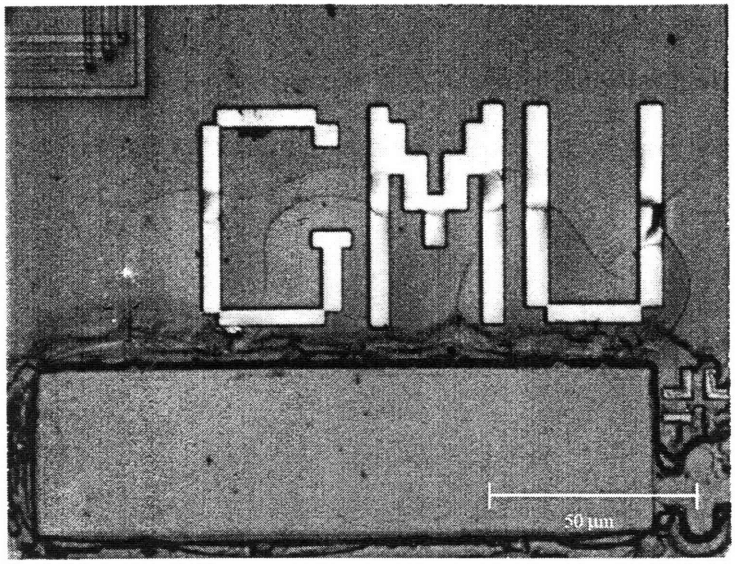

Figure 4-22. Optical microscope photograph of the OPTOCHIP which was the target substrate for Sample 41. The letters GMU indicate where the pillar contacted the surface, missing the well it was intended for.

Alignment was improved for the next sample, but another problem was discovered. The features of the OPTOCHIP were taller than first expected, and the height of the pillars, approximately 10 µm, was not tall enough. The source substrate contacted the OPTOCHIP in regions other than the pillars, leaving impressions of the OPTOCHIP features on the substrate, as shown in Figure 4-23. This prevented the pillars from bonding in the wells. Whether this is due to the fact that the pillars did not touch the bottom of the well or that the pressure was not high enough due to the larger area of contact is uncertain. The wells, shown in Figure 4-24, appear to be contaminated. This is probably due to the high temperature, 625°C, at which the sample was heated. This is sufficient to cause some vapor-phase transport, and the observed roughening of the surface may be due to the evaporation of As, or the deposition of Ga. The alignment in this sample was good. In fact, careful examination of the wells shown in Figure 4-24 show darkened areas roughly corresponding to the shape and location of the pillars, in the upper right corner of the

well. There is a V-shaped fragment of GaAs also apparent in the well on the right. This is reflected on the pillar on the source substrate, in Figure 4-25, confirming alignment.

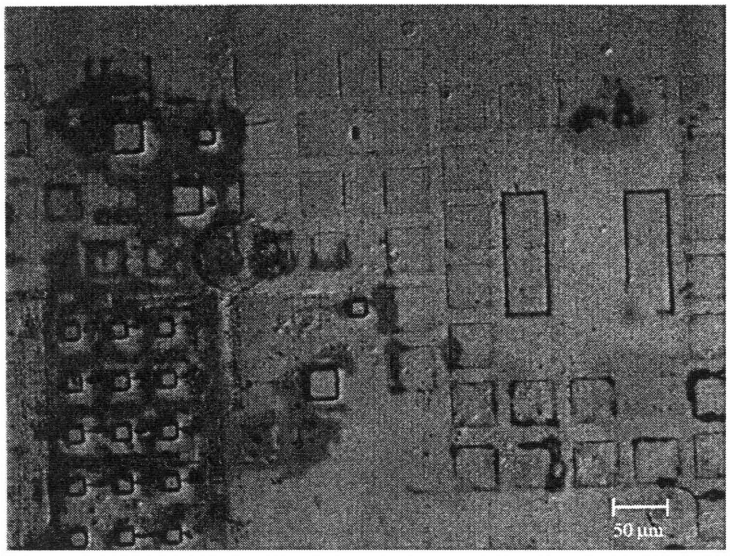

Figure 4-23. Optical microscope photograph of the source substrate for Sample 42. It shows impressions left by the OPTOCHIP's features.

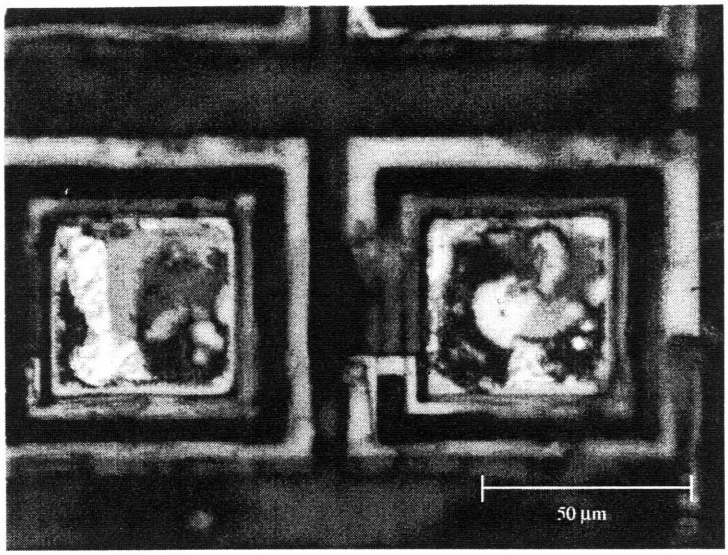

Figure 4-24. Optical microscope photograph of the wells in which pillars failed to bond, from Sample 42. The darkened areas in the upper right corner indicate the area where the pillars were. There is also a V-shaped fragment of material in the well on the right which is reflected on the pillar.

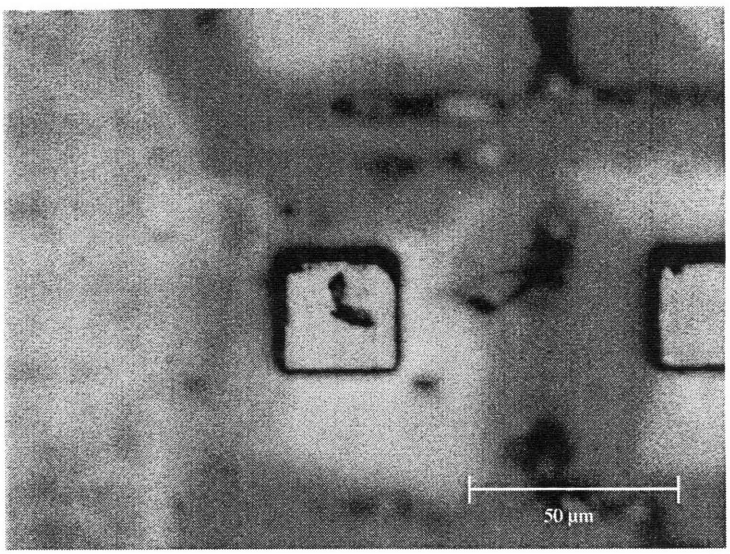

Figure 4-25. Optical microscope photograph of the pillar which was in the well on the right in the previous figure. It shows a V-shaped reflection of the fragment in the well.

The final sample, Sample 43, did bond successfully. The pillar height was increased to 15 μm, sufficient to avoid contact with the OPTOCHIP's surface, and the bonding temperature set to 530°C, low enough to avoid significant damage to the contacts or the transistors, but high enough to ensure a good bond. Figure 4-26 shows a pillar which was successfully bonded and then revealed by etching away the substrate. The pillar is small compared to the well size not only due to the PILLAR mask, which has features slightly smaller than the well, but also due to the wet etch used to complete the etching of the pillar. This should be avoidable in the future, as it was due solely to a problem with the RIE. The fact that the pillar is against one wall of the well is not surprising. The method of aligning and then transferring the sample to the bonding boat depends on the pillar being in the well to maintain alignment. Thus it would be natural that the pillar would slide to one wall of the well in the alignment process. This may be avoidable if a method which allows adhesion on initial contact is found. "Palladium bonding revisited" on page 76 contains more information on how this may be done.

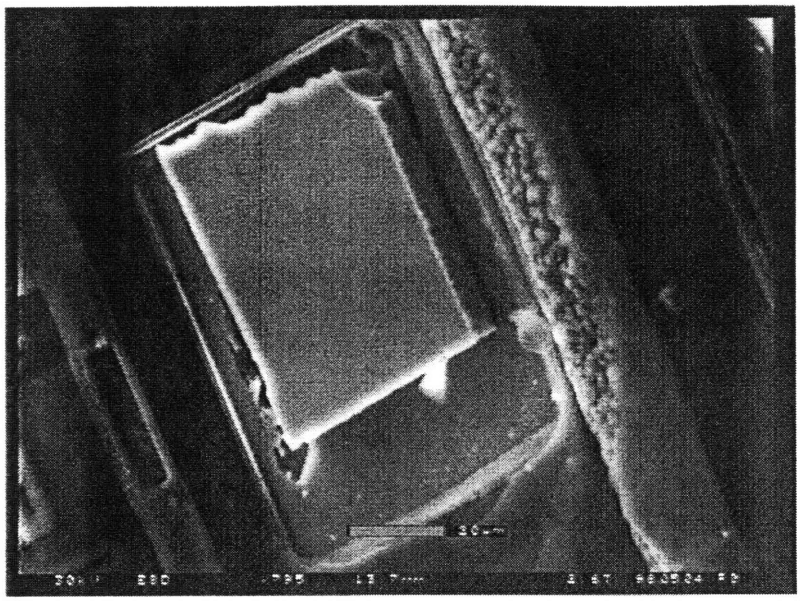

Figure 4-26. SEM image of a pillar successfully bonded into a well from Sample 43. It is flush with the side of the well. The tilt of this sample is 45°.

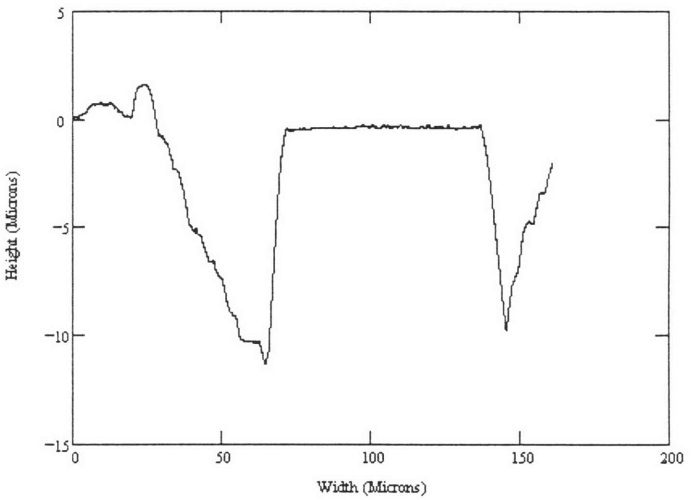

Figure 4-27. Dektak profile of the pillar in the previous figure. The sloping of the sidewalls is partially due to the limited resolution of the profiler. The walls of the pillar itself do not appear to be sloped in other observations, although those of the well are.

Deformation due to the pressure cannot be directly observed in this sample. The area at the bottom of the well is not easily probed with a Dektak tip. However, cracks in the SiO_2, apparently stemming from wells in which pillars were bonded, can be seen. The SEM photograph in Figure 4-28 shows these cracks. These were not seen prior to bonding. Cracks in the dielectric were seen in other OPTOCHIP samples with MBE grown devices, however, and may be caused by the difference in the coefficients of thermal expansion of GaAs and SiO_2. Slip in the GaAs crystal around the wells may contribute to the cracking as well.

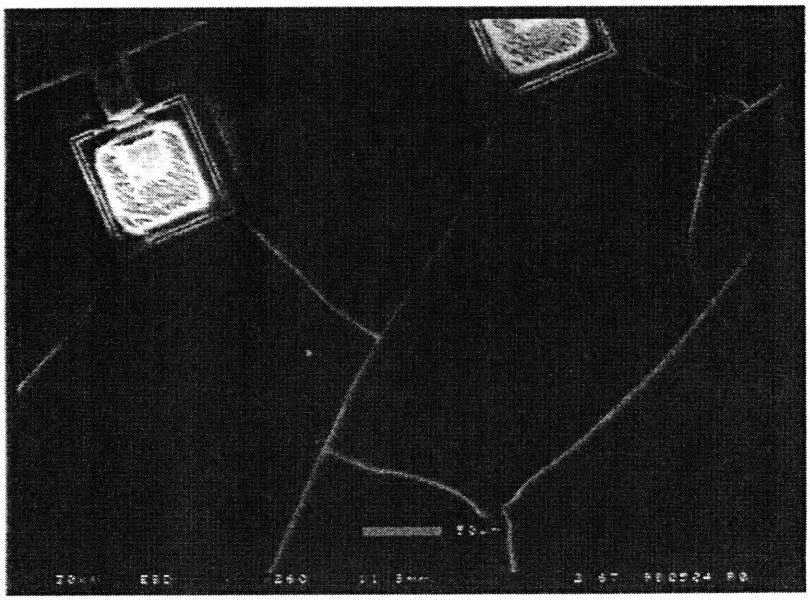

Figure 4-28. SEM image of cracks in the SiO_2 apparently stemming from some of the wells in the OPTOCHIP. These may have been caused by slip.

Chapter 5

Conclusions

5.1 Project Summary

This project has demonstrated the feasibility of aligning pillars with wells made in VLSI-fabricated GaAs substrates and bonding them there. This offers another avenue for producing optoelectronic devices, allowing the bonding of LEDs, VCSELs, QWIPs, or other heterogeneous optical devices to VLSI electronics. The devices themselves may be grown in bulk and then processed for bonding. Additional flexibility is drawn from the fact that the device may be grown on any substrate, including InP. This allows integration of devices that could not be grown on the substrate used for the electronics.

The mechanism for bonding is believed to be wafer fusion. This involves decomposition of the bonded semiconductors at their surface, and the formation of covalent bonds between the surfaces accompanying the recomposition of the material. It is possible, however, that direct bonding resulted from other forces. Van der Waals is unlikely, but hydrogen bonding on an oxide layer is a possibility. Every effort was made to avoid the formation of an oxide, but this proved very difficult to accomplish for the aligned bonding.

The greatest barrier to further work is the extreme pressure used in the bonding, which leads to an observed deformation of both the source and target substrate. The deformation has little apparent effect on the bond. None of the measurements gave any indication that the bond of the pillar is weaker or less conductive to electricity than bonding over a flat wafer, which, since it is subjected to less pressure, has less curvature. The interface now has a slightly curved, rather than a planar, surface. In heterojunctions this may have interesting effects, and the relocation of the surface defects on the curve rather than a plane may make a difference, but neither mechanical

nor electrical quality are measurably lower. It is difficult to determine how much this dislocation motion would be expected to increase the density of defects at the interface. The defects which move to the interface may in fact be reduced by the vapor and surface diffusion which take place there. The slip planes are not confined to the area over which the pillars bond: they affect a large region of the target substrate, as is readily apparent in Figure 4-17. The deformation due to slip may very well be responsible for the cracking of the SiO_2 observed on the OPTOCHIP. Another question is whether the defects produced by Frank-Read sources that exist within the bulk substrate reduce its conductivity. The J-V curves seem to indicate otherwise: the pillar bonds have better conductivity than the bonding between flat surfaces. But there are other factors in the conductivity than the deformation, such as the trapping of methanol between the flat samples. The deformation can be reduced by using a lower pressure in bonding. This was difficult with the current bonding fixture, which applies pressure to the sample with limited precision, but a different design could produce a smaller force, and a smaller pressure. This would be the preferred approach.

5.2 Devices

The OPTOCHIP project depends on the ability to place devices, not just GaAs, in these wells. Figure 5-1 shows a LED grown into a well by MBE on one of the OEICs created by the OPTOCHIP foundry. In order for wafer bonding to be a viable alternative to direct growth of the material in the wells, similar structures need to be produced and bonded.

First, it is desirable to make the structure larger. This makes alignment more difficult, but a larger area produces better optical devices. Alignment is possible within about five microns under infrared. A pillar five microns smaller than the wells on every side would be competitive with direct MBE growth, since the grown material tends to be poor around the edges of the well in any case.

The next consideration is the effect of heterogeneous structures: multilayer structures present additional difficulties. First, the different materials would not etch at the same rate in RIE, possibly requiring different etches to etch the pillar to the correct depth. Second would be the problem of different coefficients of thermal expansion. Fortunately, this would not be a problem for MBE grown materials, since they undergo the same range of temperatures during growth. Using devices which would normally need to be produced at lower temperatures may be a problem. Third, the devices would need to be grown upside-down, since it is the top layer that is bonded to the bottom of the well. This layer does not need to be GaAs, although this would provide the best electrical contact with the substrate underneath. The top layer would be best suited if it were an etch stop for the etching of the source substrate. This would allow the etching to proceed with less concern of stopping in the right place. InGaP DBRs (dielectric Bragg reflectors) used in VCSELs would work well as etch stops without the need for a specially grown layer.

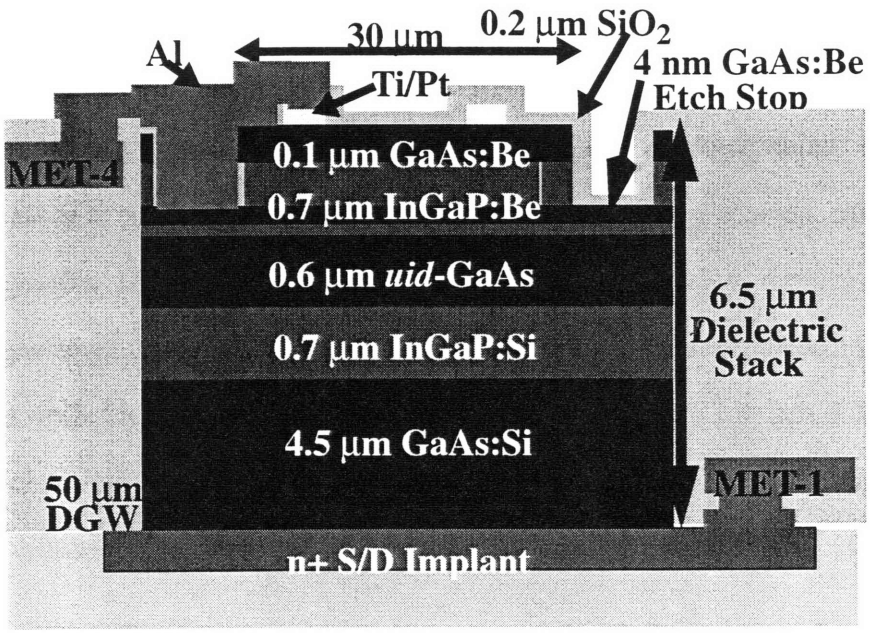

Figure 5-1. LED as grown into an OEIC well. (Courtesy of Joe Ahadian.)

5.3 Palladium bonding revisited

While palladium bonding had initially been rejected as a viable means of bonding, it should be reconsidered in future work. The high reflectivity of a palladium bond, although difficult when in an active region of an optical device, would not necessarily be a hindrance in the OPTOCHIP project. Here, the light emitting device, whether LED or VCSEL, is grown by heteroepitaxy. The bonding is not part of the formation of the device, but is used to connect the device to the electronics. Thus there is no need to transmit light through the junction. The question then

becomes not whether light can pass through the junction, but whether the palladium interferes with the operation of the device. As long as the palladium bond is separated from the device by a buffer layer, this should not be a problem.

The following process is recommended: The first step is the growth of the desired device. This is done on a bulk substrate. During the growth, an etch stop is the first layer grown to prevent the etch used to remove the substrate from etching the device. The device must be grown upside down, with the top layer being the buffer between the lower DBR and the substrate. Then the sample can be patterned. The PILLAR mask creates an inverse of the pillars by using a negative resist. Then, 1000 Å of palladium is deposited by thermal evaporation, and removed by lift-off. The amount of the palladium is one of the factors which need to be refined over the course of the experiment. This pattern of palladium is then used as a mask in the reactive ion-beam etching of the pillars to be transferred. The wafers are then aligned using the infrared backside aligner. The opaqueness of the deposited palladium, 0.8 - 0.9 reflectivity, should make the alignment easier. Once aligned, the sample can be bonded in the furnace used for wafer fusion, but at a lower temperature, 350^{o}C, and less pressure. With an etch stop, lapping is feasible, since the unevenness of the remaining material is of little concern if the etch is prevented from proceeding past the top of the pillar. The substrate can then be etched away similarly to the method used to remove the substrate in the wafer fused samples. Alternatively, a sacrificial layer would simplify the wet etch, although the selection of such a layer may be difficult. The substrate would need to be removed without damaging the underlying OPTOCHIP or the optical device.

The main advantage of this approach is that it allows strong bonding with excellent electrical properties to be done at a lower temperature and pressure than wafer fusion. It is also easier to align since the opaque Pd can be easily seen by the infrared backside aligner. Additionally, the formation of an oxide on the GaAs would not be a difficulty since Pd can easily diffuse through it. Finally, the room-temperature reaction of the Pd with the semiconductor may provide some adhesion when first contacted in the aligner. The adhesion would most likely not be immediate, and

would require leaving the samples pressed together in the aligner for some time. However, this would make it easier to transfer the sample to the furnace without destroying the alignment. It is uncertain how well this would work, however, and it would have to be demonstrated.

Appendix I

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Appendix II

Sample Database

The following pages contain a complete database of all the bonding samples. Among the information contained in the time and temperature of baking, the preparation of the samples, and the results, including I-V curves, where available.

Sample Number: 1

Date: 7/2/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

Evacuate tube for half hour w/N2
1.5 hr ramp w/H2
Bake w/H2
Cool for 2.5 hr w/N2

Time (hour: 3

Temperature (: 625

Torque (in-l:

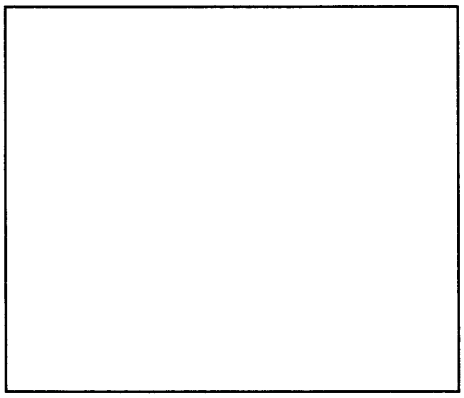
Size (mm2:

Pressure (kg/cm2):

Results

Adhered, but broke apart easily
Some mirroring a features

I-V curve



Sample Number: 2

Date: 7/9/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

Time(hour: 3

Temperature (: 625

Torque (in-l

Size (mm2

Pressure(kg/cm2)

Results

I-V curve

Sample Number: 3

Date: 7/12/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

Time (hour

Temperature (

Torque (in-l

Size (mm2

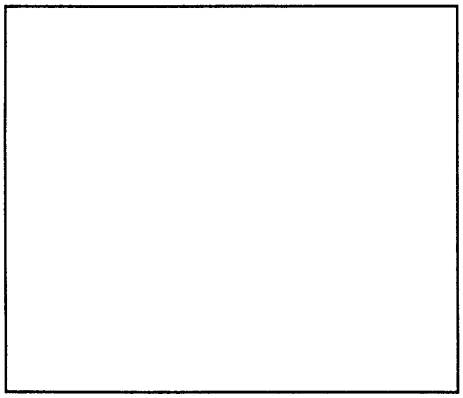
Pressure (kg/cm2)

Results

Aborted run!

Sample not bonded

I-V curve



Sample Number: 4

Date: 8/1/97

Wafer 1: p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2: p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation:
2 min etch in NH4OH
Put together in Methanol

Recipe:
.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 625

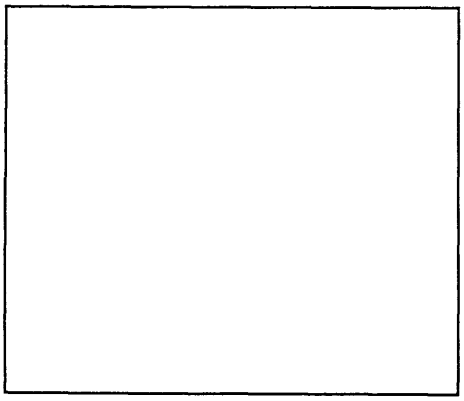
Torque (in-l

Size (mm2

Pressure(kg/cm2)

Results:
Adhered, but separated cleanly

I-V curve



Sample Number: 5

Date: 8/2/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 800

Torque (in-l

Size (mm2

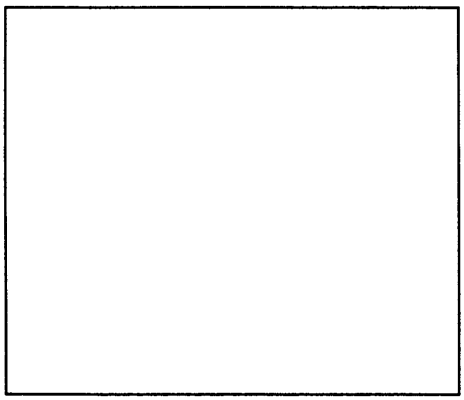
Pressure(kg/cm2)

Results

Adhered, but spotty
The samples adhered over a fairly large area: did not break cleanly

Metal contact damaged

I-V curve



Sample Number: 6

Date: 8/4/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 800

Torque (in-l: 4

Size (mm2: 8

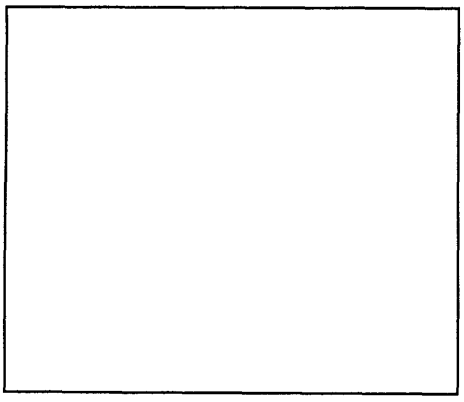
Pressure(kg/cm2): 244.6938775510

Results

Strong fusion
Cleaved w/o separating

Metal contact apparently damaged

I-V curve



Sample Number: 7

Date: 8/5/97

Wafer 1:
p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2:
p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation:
2 min etch in NH4OH
Put together in Methanol

Recipe:
.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

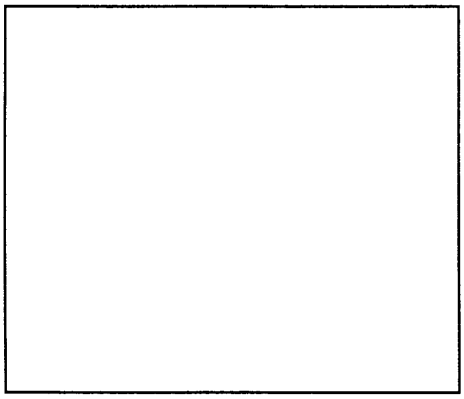
Time(hour	Temperature (
0.5	625

Torque (in-l	Size (mm2	Pressure(kg/cm2)
3	10	146.8163265306

Results:
Strong adherence: will not separate

Metal contact does not look good

I-V curve



Sample Number: 8

Date: 8/6/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

Size (mm2: 5

Pressure(kg/cm2): 293.6326530612

Results

Separated, but could see bonded over large area

I-V curve

Sample Number: 9

Date: 8/7/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time (hour: 0.5

Temperature (: 400

Torque (in-l: 3

Size (mm2: 6

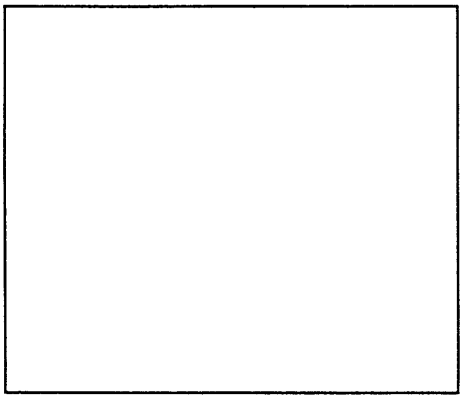
Pressure (kg/cm2): 244.6938775510

Results

Due to outages, more than one attempt made to start run before success

Identical to 8 except striped

I-V curve



Sample Number: 10

Date: 8/11/97

Wafer 1:
p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2:
p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation:
2 min etch in NH4OH
Put together in Methanol

Recipe:
.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

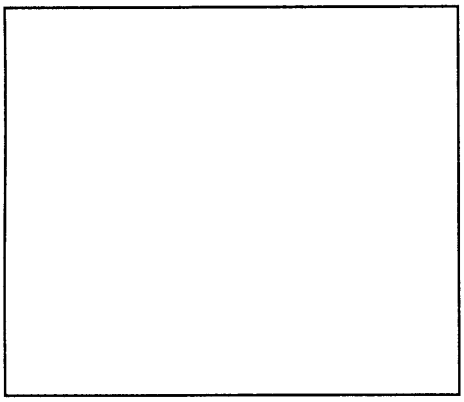
Time(hour	Temperature (
0.5	625

Torque (in-l	Size (mm2	Pressure(kg/cm2)
3	20	73.40816326530

Results:
Cleaved without separating

Metal contacts seem damaged

I-V curve



Sample Number: 11

Date: 8/12/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 800

Torque (in-l: 3

Size (mm2: 3

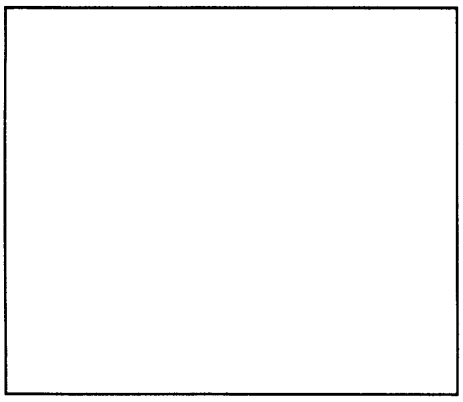
Pressure(kg/cm2): 489.3877551020

Results

Looks okay: another successful run

Metal contacts damaged, though

I-V curve



Sample Number: 12

Date: 8/13/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in NH4OH
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

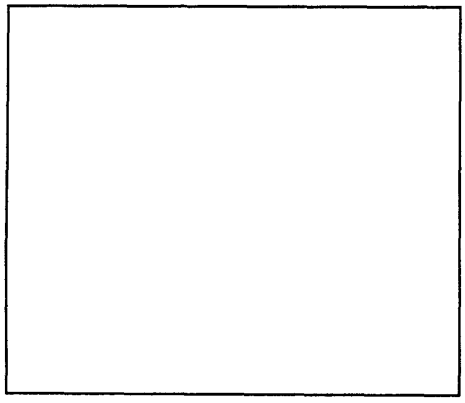
Size (mm2: 14

Pressure(kg/cm2): 104.8688046647

Results

Separated, but not cleanly -- broke first.
Note that they did not appear well aligned

I-V curve



Sample Number: 13

Date: 8/27/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

3 min etch in 7:1 BOE (NH4F:HF)
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time (hour: 0.5

Temperature (: 625

Torque (in-l: 3

Size (mm2: 22

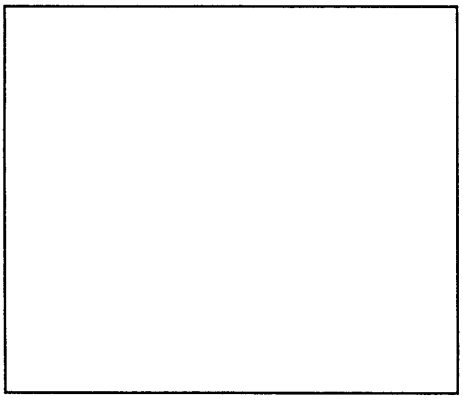
Pressure (kg/cm2): 66.73469387755

Results

Seemed to be a decent bond

Contacts do not look good

I-V curve



Sample Number: 14

Date: 8/30/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

3 min etch in 7:1 BOE (NH4F:HF)
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

Size (mm2: 6

Pressure(kg/cm2): 244.6938775510

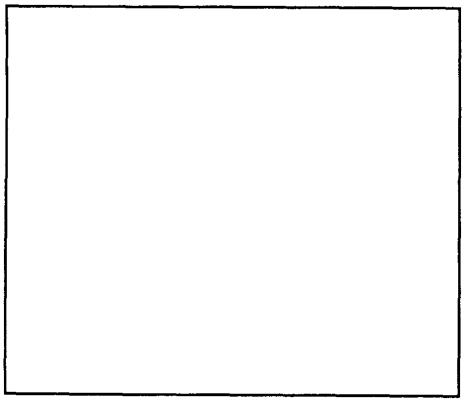
Results

Separated afterwards, spotty bonding

Shows interesting stripes

Okay contact

I-V curve



Sample Number: 15

Date: 9/1/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

3 min etch in 7:1 BOE (NH4F:HF)
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 800

Torque (in-l: 3

Size (mm2: 13

Pressure(kg/cm2): 112.9356357927

Results

Good bond

Bad contact

I-V curve

Sample Number: 16

Date: 9/3/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

Size (mm2: 20

Pressure(kg/cm2): 73.40816326530

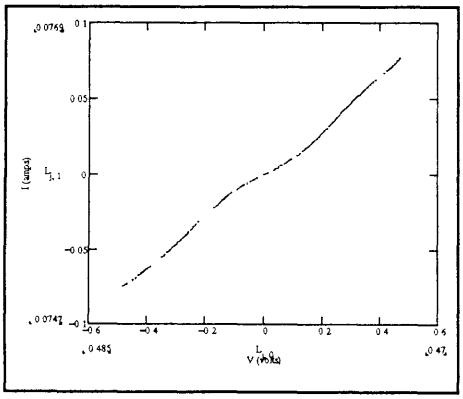
Results

Good bond: cleaved without separating

Good contact

Have electrical characteristics

I-V curve



Sample Number: 17

Date: 9/6/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 625

Torque (in-l: 3

Size (mm2:

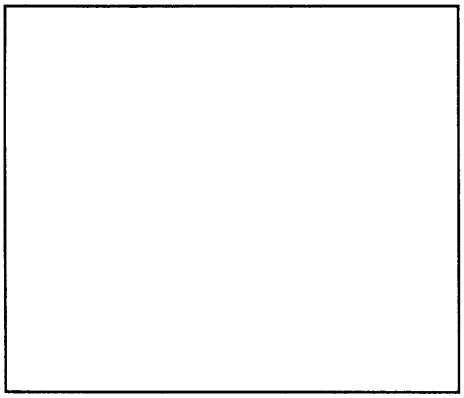
Pressure(kg/cm2):

Results

Good bond

Bad contact

I-V curve



Sample Number: 18

Date: 9/8/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 800

Torque (in-l: 3

Size (mm2: 12

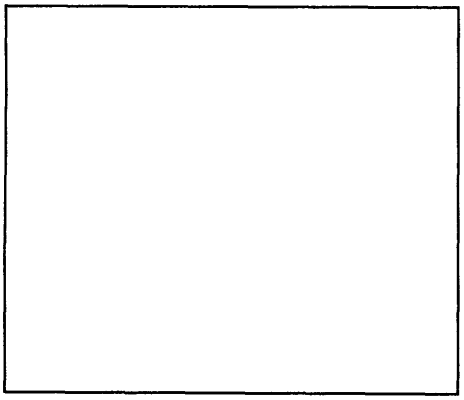
Pressure(kg/cm2): 122.3469387755

Results

Good bond

Bad contact

I-V curve



Sample Number: 19

Date: 9/25/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

Size (mm2: 3

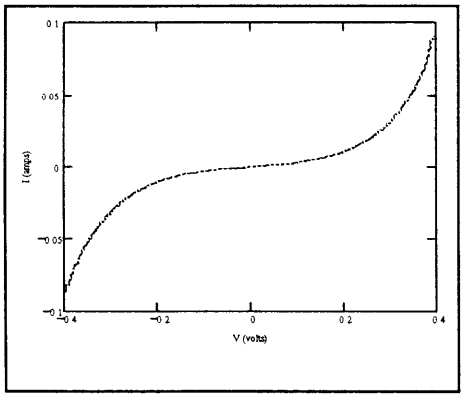
Pressure(kg/cm2): 489.3877551020

Results

Does not separate, but poor alignment
High resistance -- very non-linear, almost diode (symmetrical about V=0)

Good contact

I-V curve



Sample Number: 20

Date: 10/1/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol (poor alignment, over-exposed to atmosphere)

Recipe

.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2 (not purified)
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

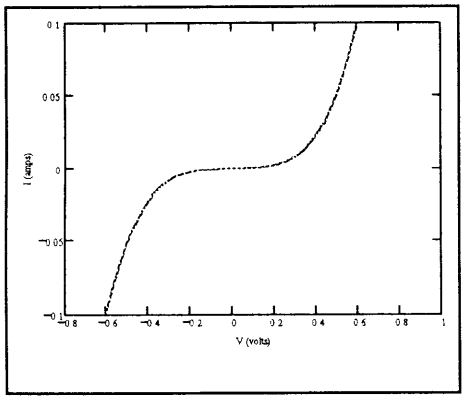
Size (mm2: 5

Pressure(kg/cm2): 293.6326530612

Results

Separated fairly easily except for one part, which stayed when rest stayed on, then shattered when removed
Stripes on contact and surface in small area on both wafers, perpendicular to resistant piece

I-V curve



Sample Number: 21

Date: 10/5/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

1.5 hour purge w/N2
0.5 hour ramp to bake temperature w/N2
Bake w/H2 (not purified)
Cool

Time(hour: 0.5

Temperature (: 500

Torque (in-l: 3

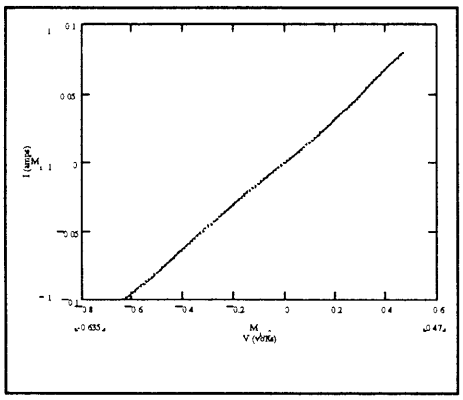
Size (mm2: 3

Pressure(kg/cm2): 489.3877551020

Results

Poorly aligned.
Would not separated.
Contact okay, but not great. I-V measurement generally sporadic, but linear when good.

I-V curve



Sample Number: 22

Date: 10/6/97

Wafer 1

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

2 min etch in 4:1 H2O:HF
Put together in Methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

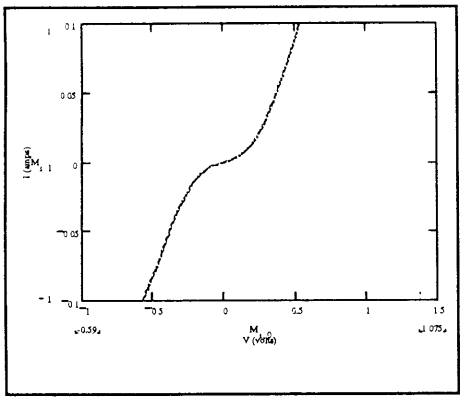
Size (mm2: 10

Pressure(kg/cm2): 146.8163265306

Results

Poor alignment.
Broke apart except for piece left behind (about 1/3rd)
Contact good

I-V curve



Sample Number: 23

Date: 11/4/97

Wafer 1

Unknown GaAs with 3.5 micron deep pillars etched with CM mask
Etch in 5:1:1 H2O:HPO3:H2O2

Wafer 2

p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation

Etch wafer 1 in NH4OH for 1 min
Etch wafer 2 in 4:1 H2O:HF for 1 min
Put together in methanol

Recipe

.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 400

Torque (in-l: 3

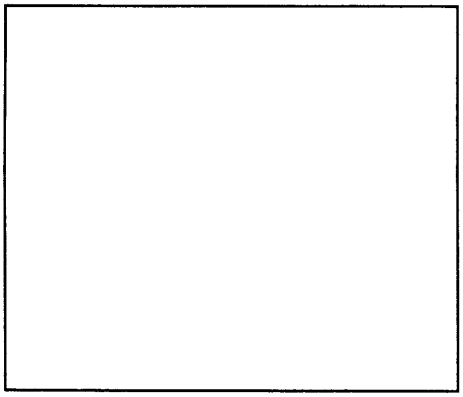
Size (mm2:

Pressure(kg/cm2):

Results

Good alignment: broke apart easily
Very high pressure -- deformed surface of GaAs

I-V curve



Sample Number: 24

Date: 11/6/97

Wafer 1:
Unknown GaAs with 3.5 micron deep pillars etched with CM mask
Etch in 5:1:1 H2O:HPO3:H2O2

Wafer 2:
p-GaAs: G7H6Z0013006 (AuTi ohmic contact on the back, and is protected by SiO2 on the front)

Preparation:
Etch wafer 1 in NH4OH for 1 min
Etch wafer 2 in 4:1 H2O:HF for 1 min
Put together in methanol

Recipe:
2 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 625

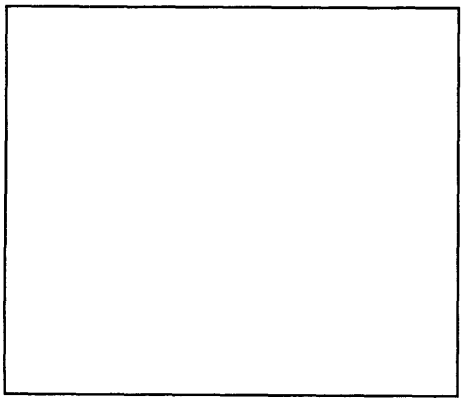
Torque (in-l: 3

Size (mm2:

Pressure(kg/cm2):

Results:
Fusion at mesas
Deformed GaAs

I-V curve



Sample Number: 25

Date: 11/13/97

Wafer 1:
G7H6Z00113006 etched with 0.6 micron mesas from CM mask (AuTi ohmic contact on the back)

Wafer 2:
G7H6Z00113006 plain wafer (AuTi ohmic contact on the back

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
2 min etch NH4OH
Put together in Methanol

Recipe:
0.5 hour purge w/N2
1 hour ramp to bake
temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 25

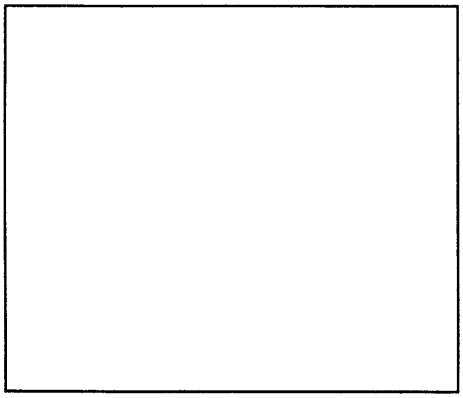
Torque (in-l: 3

Size (mm2:

Pressure(kg/cm2):

Results:
No fusion (although a few spots are visible)
No deformation

I-V curve



Sample Number: 26

Date: 11/20/97

Wafer 1

G7H6Z00113006 etched with 0.6 micron mesas from CM mask (AuTi ohmic contact on the back)

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
2 min etch NH4OH
Put together in Methanol

Recipe

0.5 hour purge w/N2
1 hour ramp to bake temperature w/N2
Bake w/H2
Cool w/N2

Time(hour: 0.5

Temperature (: 625

Torque (in-l:

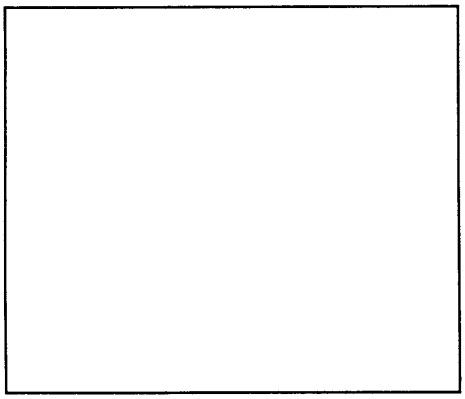
Size (mm2:

Pressure(kg/cm2):

Results

Used cap and wafer to apply pressure
No bonding, no deformation of substrate

I-V curve



Sample Number: 27

Date: 12/19/97

Wafer 1

G7H6Z00113006 etched with 0.6 micron mesas from CM mask (AuTi ohmic contact on the back)

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
2 min etch NH4OH for wafer 1
2 min etch 4:1 H2O:HF for wafer 2
Put together in Methanol

Recipe

1.5 hour N2 purge
1 hour ramp w/ H2
Bake w/ H2
0.5 hour ramp down w/ H2
0.5 hour cool w/ H2
2 hour cool w/ N2

Time (hour: 0.5

Temperature (: 625

Torque (in-l: 0.3

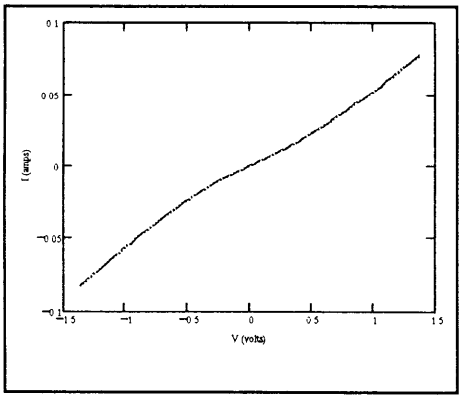
Size (mm2:

Pressure (kg/cm2):

Results

Screws finger tight
Ridges of unetched material around edges: not just pillars
Holds together fairly well: evidence of good adhesion (uprooted bits)
No evidence of deformation

I-V curve



Sample Number: 28

Date: 1/13/98

Wafer 1

G7H6Z00113006 etched with 0.6 micron mesas from CM mask (AuTi ohmic contact on the back)

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
2 min etch NH4OH for wafer 1
2 min etch 3:1 H2O:HF for wafer 2
Put together in Methanol

Recipe

.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

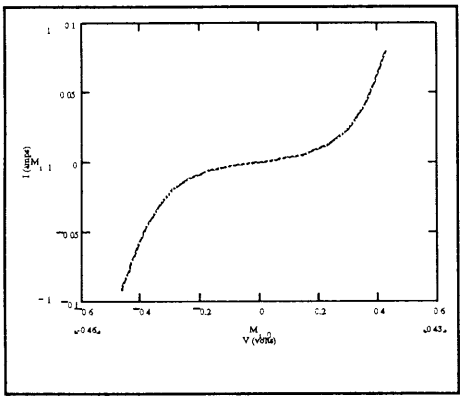
Time(hour	Temperature (
0.5	450

Torque (in-l	Size (mm2	Pressure(kg/cm2)
0.3	0.43	341.4333175130

Results

Good adhesion, especially around edges of pillars
Apparent deformation

I-V curve



Sample Number: 29

Date: 1/25/98

Wafer 1

MBE growth #9373 (6 um p-GaAs/1000 A AlAs/ p-GaAs substrate) RIE etched 8 um pillars

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 for 2 min in NH4OH
Etched wafer 2 for 2 min in 4:1 HF:H2O

Recipe

.5 hour N2 purge
0.5 hour ramp w/ N2
0.5 h ramp w/H2
Bake w/ H2
1.5 hour ramp down w/ H2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 625

Torque (in-l: 0.3

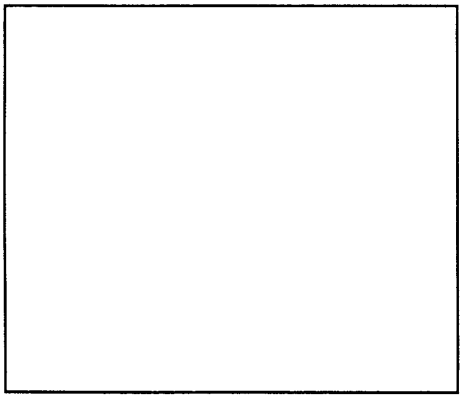
Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results

Good adhesion
Etched off sacrificial layer, some pillars left behind
Low yield ~ 5%

I-V curve



Sample Number: 30

Date: 1/28/98

Wafer 1

G7H6Z00113006 wafer (AuTi ohmic contact on the back, SiO2 on front)--RIE etched 4? um pillars

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 for 2 min in NH4OH
Etched wafer 2 for 2 min in 4:1 HF:H2O

Recipe

.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 450

Torque (in-l: 0.3

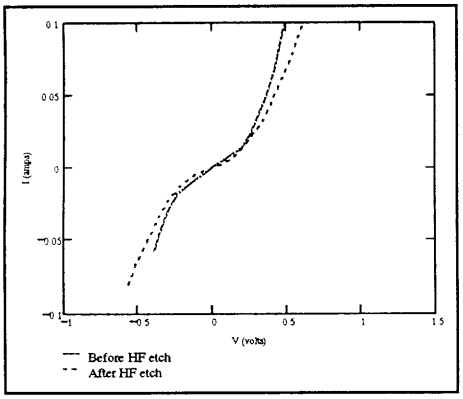
Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results

Good adhesion
Etched with HF after bonding to test bond endurance--effect on conductivity shown in I-V curve

I-V curve



Sample Number: 31

Date: 2/1/98

Wafer 1

MBE growth #9373 (6 um p-GaAs/1000 A AlAs/ p-GaAs substrate) RIE etched 4 um pillars

Wafer 2

G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation

Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 for 2 min in NH4OH
Etched wafer 2 for 2 min in 4:1 HF:H2O

Recipe

.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 450

Torque (in-l: 0.3

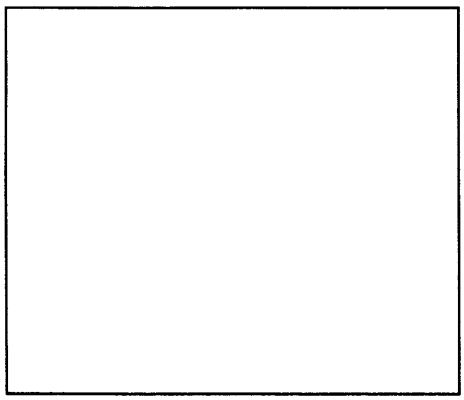
Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results

Poor adhesion

I-V curve



Sample Number: 32

Date: 2/3/98

Wafer 1:
MBE growth #9373 (6 um p-GaAs/1000 A AlAs/ p-GaAs substrate) RIE etched 4 um pillars

Wafer 2:
G7H6Z00113006 plain wafer (AuTi ohmic contact on the back, SiO2 on front)

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 for 2 min in NH4OH
Etched wafer 2 for 2 min in 4:1 HF:H2O

Recipe:
.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 450

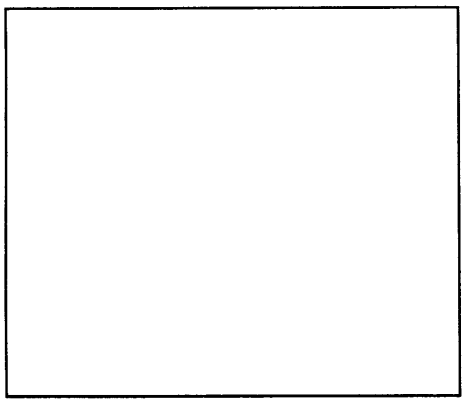
Torque (in-l: 0.3

Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results:
Poor adhesion

I-V curve



Sample Number: 33

Date: 3/7/98

Wafer 1:
Growth 9373: Patterned and RIE for 60 min at 25 T and 150 W for 11-15 um pillars
Etch off SiO2 in RIE

Wafer 2:
Plain wafer from G7H6Z001300-19

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 and wafer 2 for 2 min in NH4OH

Recipe:
.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 625

Torque (in-l: 0.3

Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results:
Good adhesion
Sacrificial etch: poor yield
Maybe not all SiO2 removed from Wafer 1

I-V curve

Sample Number: 34

Date: 3/14/98

Wafer 1:
Growth 9373: Patterned and RIE for 60 min at 25 T and 150 W for 11-15 um pillars
Etch off SiO2 in RIE; etch remaining SiO2 in BOE

Wafer 2:
Plain wafer from G7H6Z001300-19

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 and wafer 2 for 2 min in NH4OH

Recipe:
.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time(hour: 0.5

Temperature (: 800

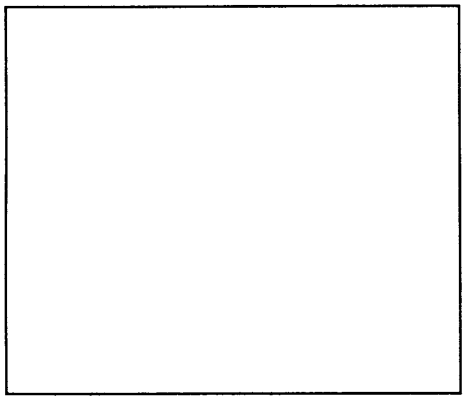
Torque (in-l: 0.3

Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results:
1 pattern
Good adhesion
Unable to do sacrificial etch: substrate will not come off
Later separates
Pillar transfer yield of 72/106

I-V curve



Sample Number: 35

Date: 3/17/98

Wafer 1:
Growth 9373: Patterned and RIE for 60 min at 25 T and 150 W for 11-15 um pillars
Etch off SiO2 in RIE; etch remaining SiO2 in BOE

Wafer 2:
Plain wafer from G7H6Z001300-19

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 and wafer 2 for 2 min in NH4OH

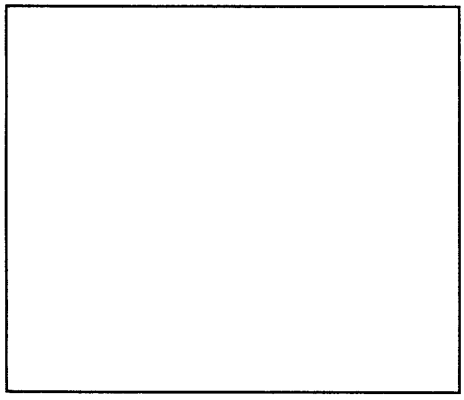
Recipe:
.5 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
1.5 hour ramp down w/ N2
1.5 hour cool w/ N2

Time (hour	Temperature (
0.5	625

Torque (in-l	Size (mm2	Pressure (kg/cm2)
0.3	0.43	341.4333175130

Results:
Good adhesion
Sacrificial etch gives good yield
Pillar transfer yield of 97/160

I-V curve



Sample Number: 36

Date: 3/18/98

Wafer 1:
Growth 9373: Patterned and RIE for 60 min at 25 T and 150 W for 11-15 um pillars
Etch off SiO2 in RIE; etch remaining SiO2 in BOE

Wafer 2:
Plain wafer from G7H6Z001300-19

Preparation:
Solvent clean: 5 min ultrasound TCE, Ace, Methanol
Etched wafer 1 and wafer 2 for 2 min in NH4OH

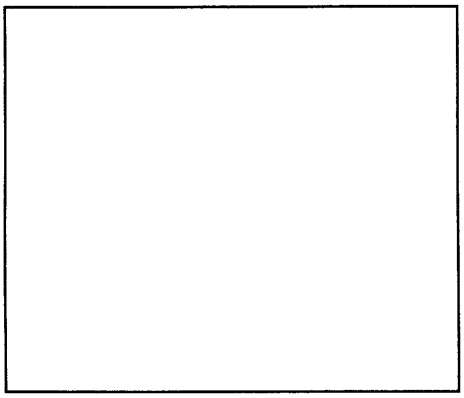
Recipe:
1 hour N2 purge
1 hour ramp w/ N2
Bake w/ H2
.5 hour ramp down w/ H2
1.5 hour cool w/ N2

Time(hour	Temperature (
0.5	450

Torque (in-l	Size (mm2	Pressure(kg/cm2)
0.3	0.43	341.4333175130

Results:
No adhesion

I-V curve



Sample Number: 37

Date: 3/31/98

Wafer 1:
RIE etched from 9373
10 um pillar (60 min etch at 150 W)

Wafer 2:
Flat wafer from G7H6Z001300-19

Preparation:
Solvent clean: 5 min ultrasound TCE, Acetone, Methanol
Wafer 1 etched in pure HF for 5 min
Wafer 2 etched in pure HF for 2 min
Put together in Methanol

Recipe:
.5 hour N2 purge
1 hour ramp w/N2
Bake w/H2
50 min ramp down w/H2
100 min ramp down w/N2
30 min cool down w/N2

Time(hour: 0.5

Temperature (: 625

Torque (in-l: 0.3

Size (mm2: 0.43

Pressure(kg/cm2): 341.4333175130

Results:
Bonded Well
Lapped afterwards -- not much taken off
Etched in 5:1:1 Water:Phosphoric:Peroxide

I-V curve

Sample Number: 38

Date: 4/2/98

Wafer 1:
RIE etched from 9373
10 um pillar (60 min etch at 150 W)

Wafer 2:
Flat wafer from G7H6Z001300-19

Preparation:
Ultrasound solvent clean both TCE, Acetone, Methanol
Wafer 1 etched in pure HF for 5 min
Wafer 2 etched in pure HF for 2 min
Put together in Methanol

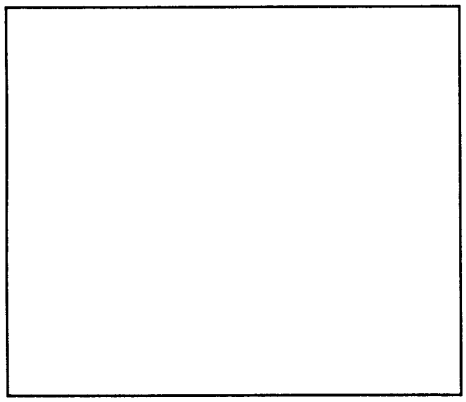
Recipe:
.5 hour N2 purge
1 hour ramp w/N2
Bake w/H2
150 min ramp down w/N2
30 min cool down w/N2

Time(hour	Temperature (
0.5	625

Torque (in-l	Size (mm2	Pressure(kg/cm2)
0.3	0.43	341.4333175130

Results:
Bonded Well
Lapped afterwards -- too far, exposed lower substrate in sections

I-V curve



Sample Number: 39

Date: 4/8/98

Wafer 1:
RIE etched from 9373
9-12 um pillar (60 min etch at 150 W)

Wafer 2:
Flat wafer from G7H6Z001300-19

Preparation:
Ultrasound solvent clean both TCE, Acetone, Methanol
Both wafers given 30 s HF dip
Put together in Methanol

Recipe:
.5 hour N2 purge
1 hour ramp w/N2
Bake w/H2
0.5 hour ramp down w/H2
1 hour ramp down w/N2
1.5 hour cool down w/N2

Time (hour: 0.5

Temperature (: 625

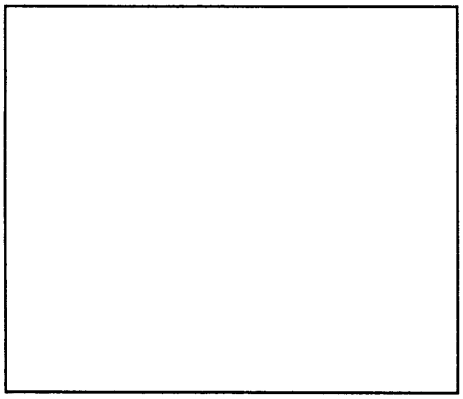
Torque (in-l: 0.3

Size (mm2: 0.43

Pressure (kg/cm2): 341.4333175130

Results:
Bonded Well
Lapped afterwards -- pretty good
Flowed resist in between
Etched with 5:1:1 Water:Phosphoric:Peroxide
Broke through unevenly -- etched through some pillars before exposing others

I-V curve



Sample Number: 40

Date: 4/17/98

Wafer 1:
RIE etched from 9373
9-12 um pillar (60 min etch at 150 W)

Wafer 2:
Flat wafer from G7H6Z001300-19

Preparation:
Ultrasound solvent clean both TCE, Acetone, Methanol
Both wafers given 30 s HF dip
Put together in Methanol

Recipe:
.5 hour N2 purge
1 hour ramp w/N2
Bake w/H2
1.5 hour ramp down w/N2
1.5 hour cool down w/N2

Time (hour: 0.5

Temperature (: 625

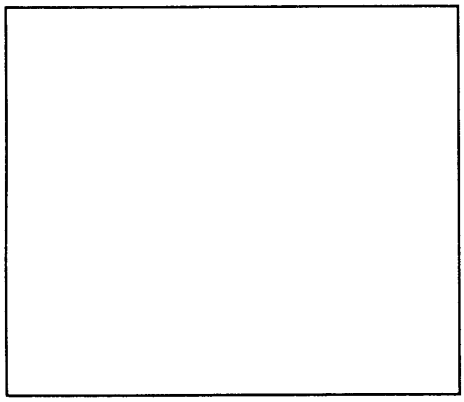
Torque (in-l:

Size (mm2: 0.43

Pressure (kg/cm2): 0

Results:
Used weight of cap and lid for pressure: not enough
Did not bond at all

I-V curve



Sample Number: 41

Date: 4/18/98

Wafer 1:
RIE etched 9-12 um pillars on plain n-GaAs wafer

Wafer 2:
Optochip, well-cleaned

Preparation:
Ultrasound solvent clean both TCE, Acetone, Methanol
Wafer 1 etched 2 minute in HF
Wafer 2 given 5 s BOE dip
Rinsed in Methanol

Recipe:
0.5 hour purge w/N2
1 hr ramp w/N2
Bake w/H2
1.5 hour ramp down w/N2

Time (hour: 5

Temperature (: 470

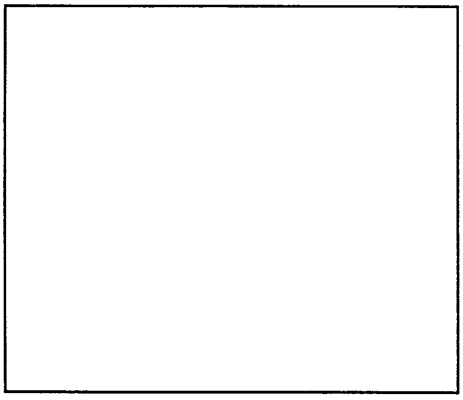
Torque (in-l: 0.1

Size (mm2: 0.39

Pressure (kg/cm2): 125.4840397697

Results:
Aligned in air prior to bonding
Knocked out of alignment (did not release from plate properly)
No bonding

I-V curve



Sample Number: 42

Date: 4/21/98

Wafer 1:
RIE etched 9-12 um pillars on plain n-GaAs wafer

Wafer 2:
Optochip, well-cleaned

Preparation:
Ultrasound solvent clean both TCE, Acetone, Methanol
Wafer 1 etched 2 minute in HF
Wafer 2 given 5 s BOE dip
Rinsed in Methanol

Recipe:
0.5 hour purge w/N2
1 hr ramp w/N2
Bake w/H2
1.5 hour ramp down w/N2

Time(hour: 0.5

Temperature (: 625

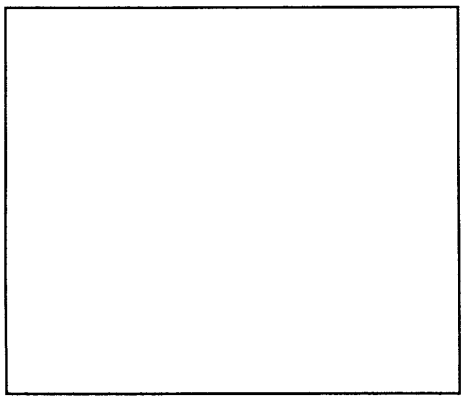
Torque (in-l: 0.3

Size (mm2: 0.39

Pressure(kg/cm2): 376.4521193092

Results:
Aligned in air prior to bonding
Did not bond
Optochip left impressions on source substrate: pillars not tall enough

I-V curve



Sample Number: 43

Date: 4/28/98

Wafer 1

n-GaAs: Etched 12 um pillars by RIE (3 hrs)
Etched 3 um by 5:1:1 H3PO4:H2O2:H2O

Wafer 2

Optochip, well-cleaned

Preparation

Solvent clean both in TCE, Acetone, Methanol
Wafer 1 etched 2 minute in HF
Wafer 2 given 5 s BOE dip
Rinsed in Methanol

Recipe

0.5 hour purge w/N2
1 hr ramp w/N2
Bake w/H2
1.5 hour ramp down w/N2

Time(hour: 3

Temperature (: 530

Torque (in-l: 0.3

Size (mm2: 0.39

Pressure(kg/cm2): 376.4521193092

Results

Aligned and bond
It worked
Good bond, alignment good
Flowed resist between wafers and wet etched: worked fairly well
Some difficulty due to uneven etch

I-V curve